

Tesla
Schematics Document

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

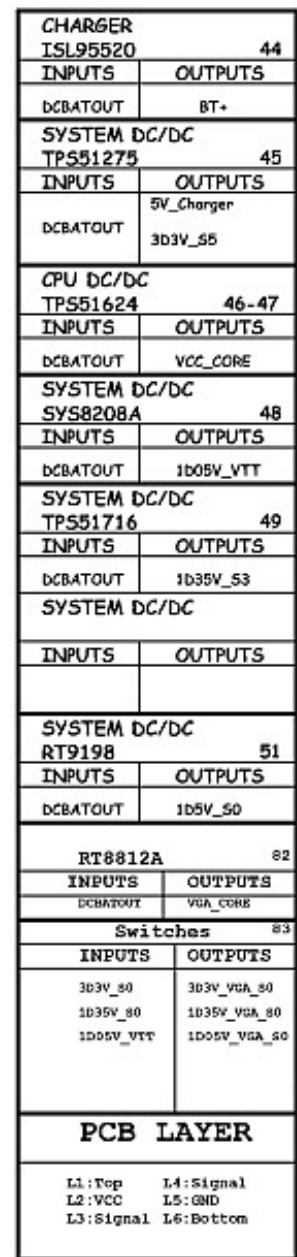
Document Number
LT41

Rev
-1

Date: Tuesday, January 20, 2015

Sheet 1 of 102

Project code : 4PD03N010001
PCB P/N : 14217



 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wei Rd., Hsinchu, Taiwan 30001, Taiwan, R.O.C.			
File			
Block Diagram			
Item	Description / Remark		Rev
	LT41		-1
Date	10/23/2015		Rev
	Drawn	2	10/23/2015

RESISTOR

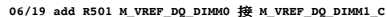
Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

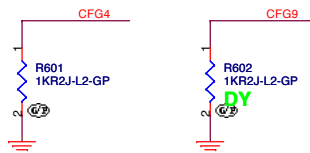
Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

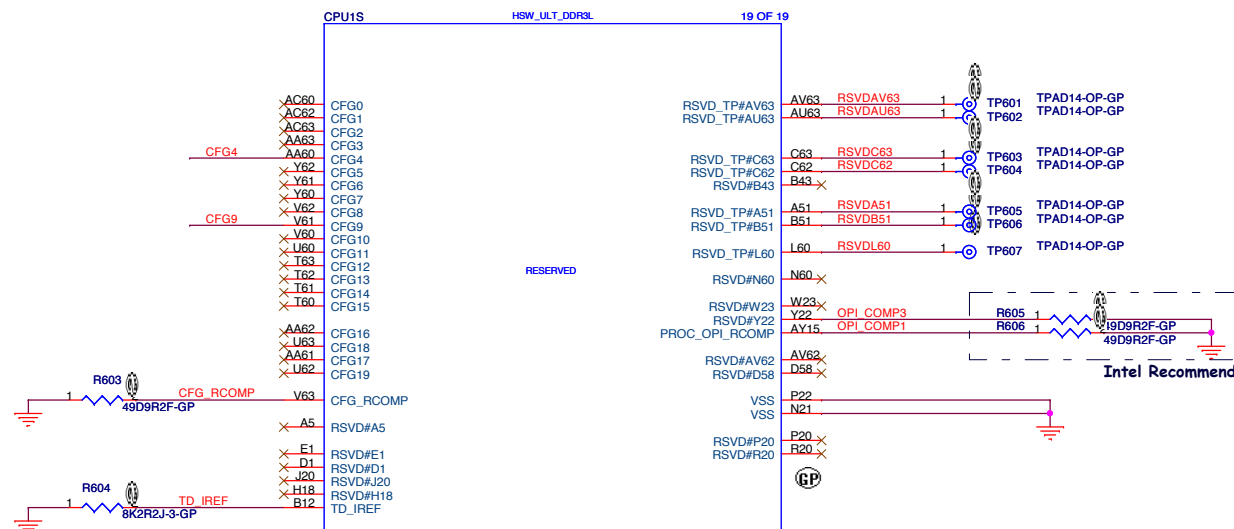


SSID = CPU

eDP Enable	1:Disable
CFG4	0:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.PCI Express* Static x16 Lane Numbering Reversal.——• CFG[4]: eDP enable<ul style="list-style-type: none">1 = Disabled0 = Enabled[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	—
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	—
continued...		



71.HASWE.G0U

HASWELL-6-GP-U

CFG9:

CPU BOM CTRL

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT
0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

HARRIS_BEACH_REFRESH

REV 0.7

PBA: G52502-004

7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

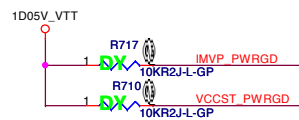
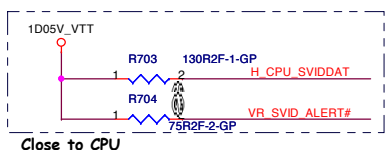
BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (CFG)			
Size	Document Number		Rev
Custom	LT41		-1
Date: Tuesday, January 20, 2015		Sheet 6 of	102

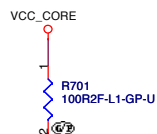
SSID = CPU

08/06 Change PG701~PG706 Close GAP

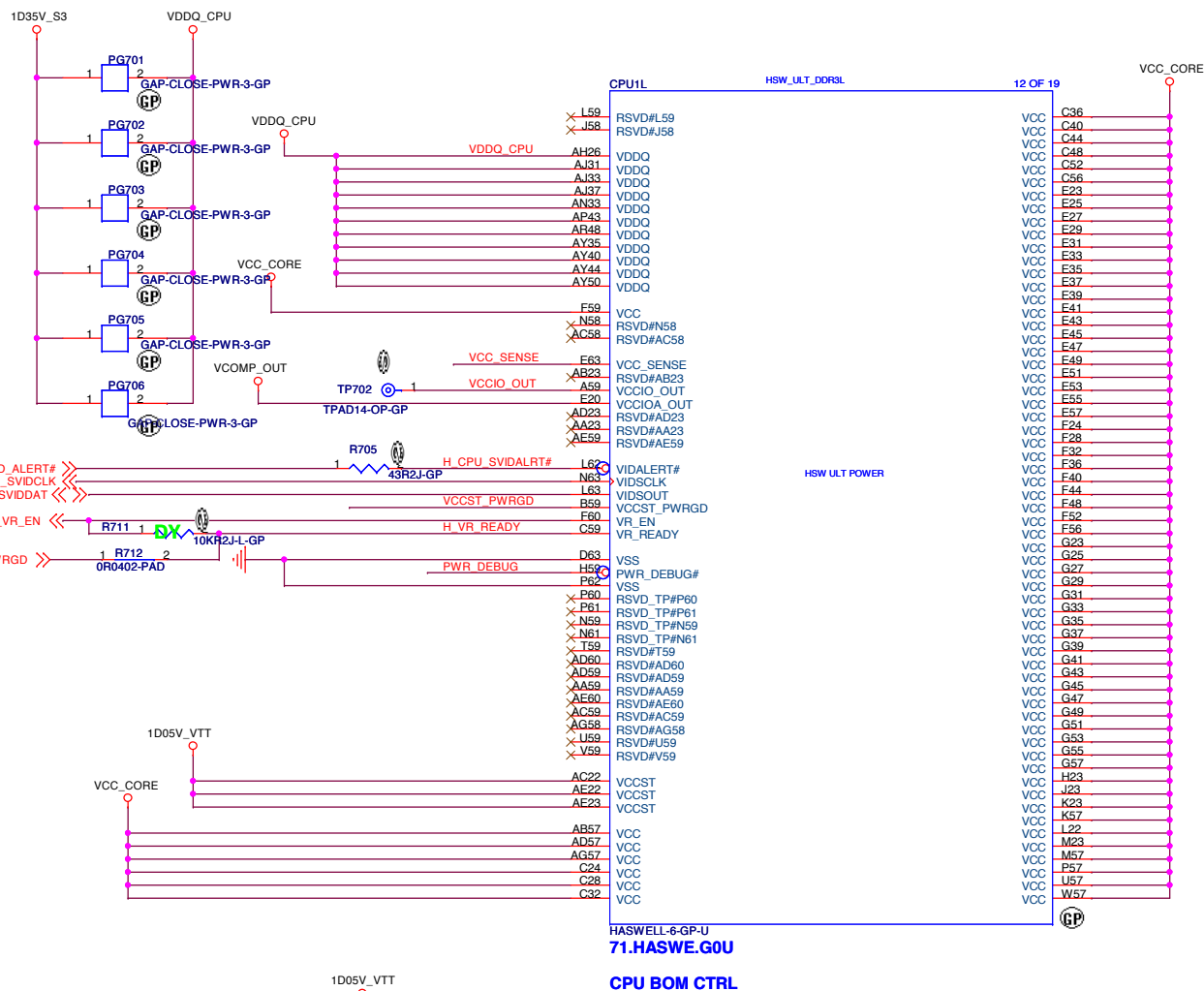
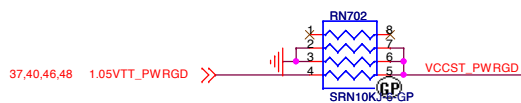
12/11 PG701-PG706 Change Part number
ZZ.CLOSE.001(上綠漆)



Follow Intel CRB



R901 close to CPU



SA
C703,C715放置AC22 AE22 AE23

SSID = CPU

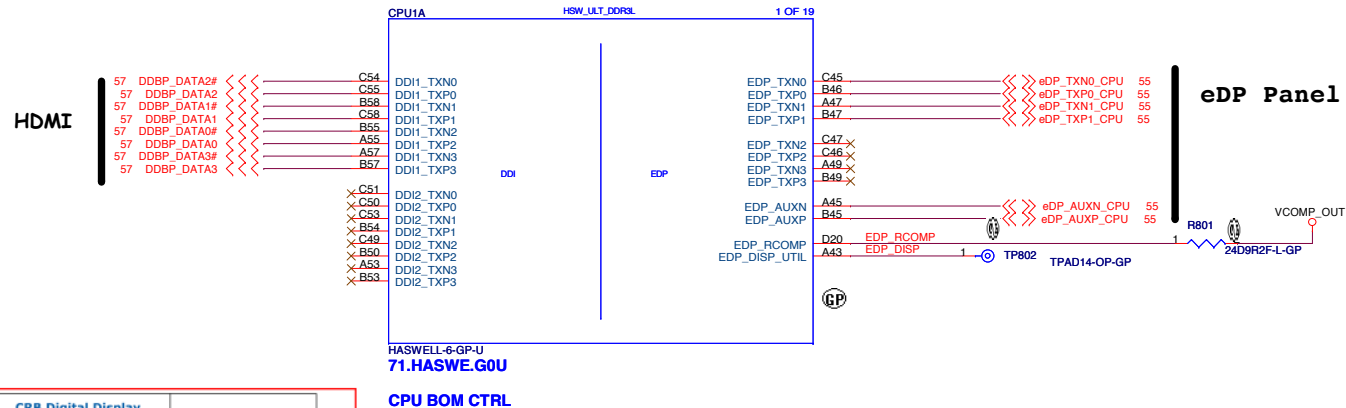


Table 19-1. Mapping of HDMI* signals for DDI ports

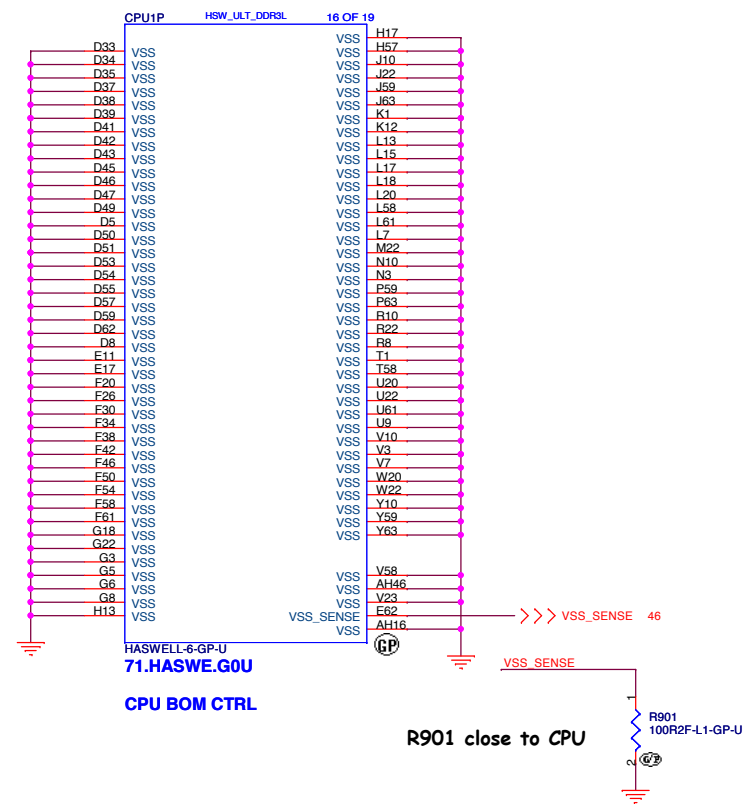
Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
Port 2	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK
		DDPB_CTRLDATA	DDI1_CTRL_DATA
	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
Port 2	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CLK
		DDPC_CTRLDATA	DDI2_CTRL_DATA

WWW.ALISALER.COM

BOM1

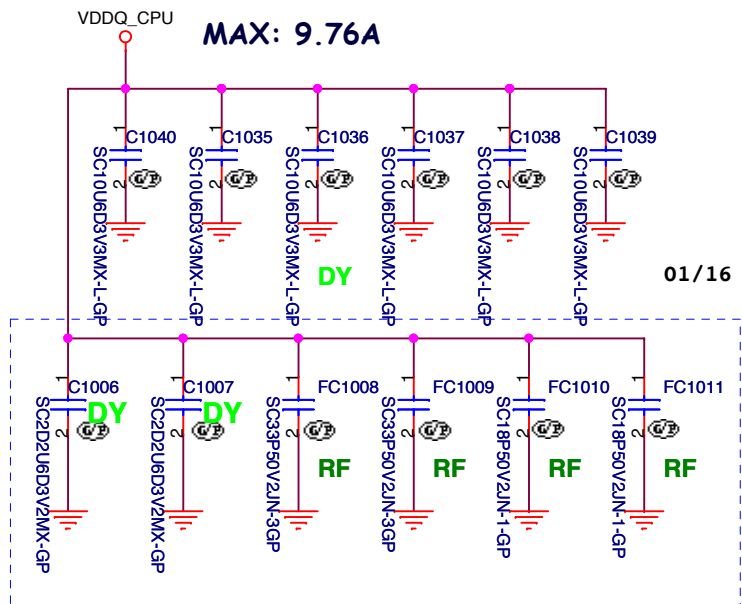
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (DDI/EDP)	
Size Custom	Document Number LT41
Date: Tuesday, January 20, 2015	Sheet 8 of 102
Rev -1	

SSID = CPU



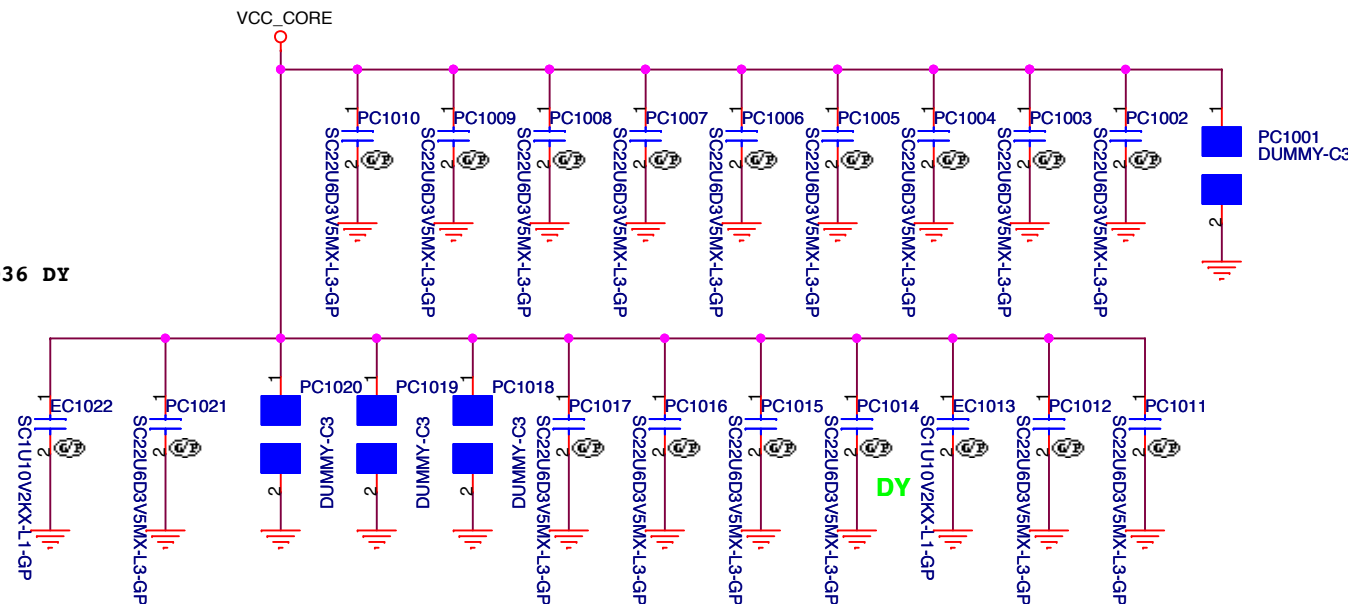
WWW.ALISALER.COM

BOM1		緯創資通 Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CPU (VSS)	
Size A3	Document Number	LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 9	of 102	



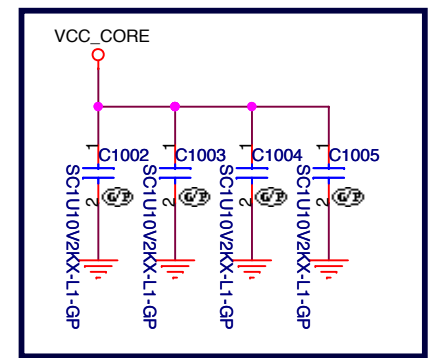
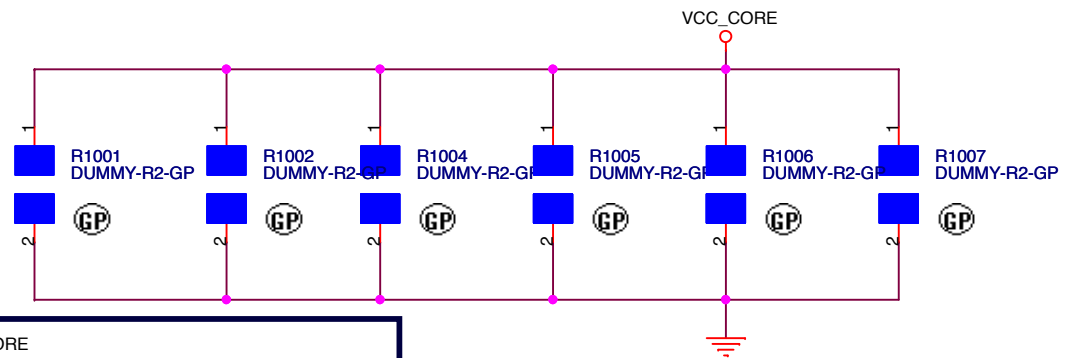
MAX: 9.76A

01/16 C1036 DY

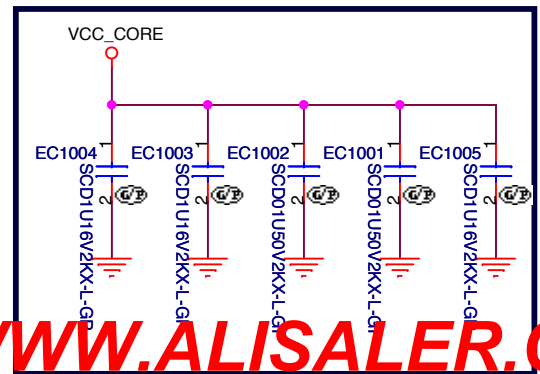


For Intel Recommend EE Part
 10/19 Change C1008, C1009 to RC1008, RC1009 (2.2uF to 33pF)
 10/19 add RC1010, RC1011 18pF

12/18 PC1013 改為EC1013 FOR EMI, 1uF 上件
 12/18 PC1022 改為EC1022 FOR EMI, 1uF 上件



For Intel Recommend EE Part



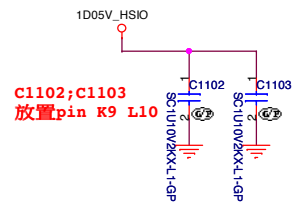
For FMC Recommend

WWW.ALISALER.COM

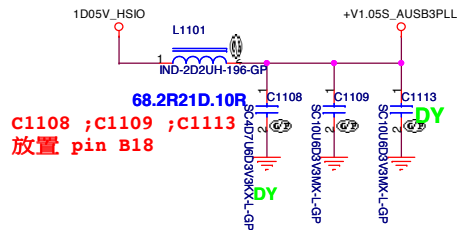
BOM1		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CPU (Power CAP1)		
Size	Document Number	Rev
A4	LT41	-1
Date:	Tuesday, January 20, 2015	Sheet 10 of 102

擺放電容的位置請參考Page 21
每個位置如下

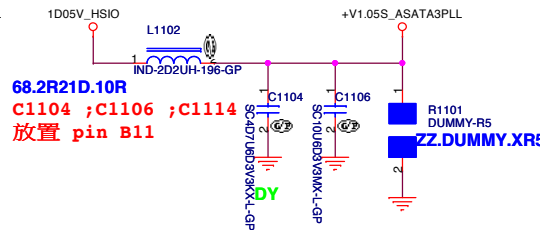
MAX: 1.92A



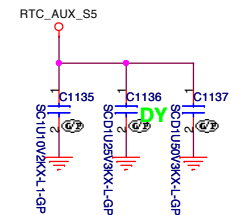
C1102;C1103
放置 pin K9 L10



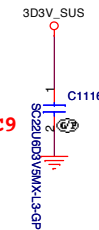
C1108 ;C1109 ;C1113
放置 pin B18



C1104 ;C1106 ;C1114
放置 pin B11



C1116放置 pin AC9

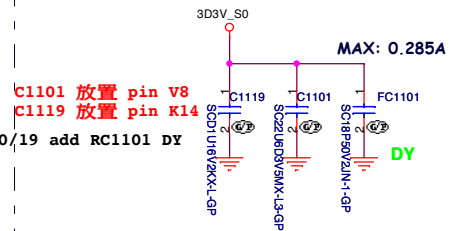


01/16 C1108 DY

01/16 C1104 DY

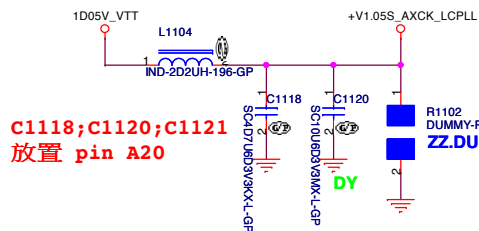
C1135;C1136;C1137
放置 pin AG10

MAX: 3.51A

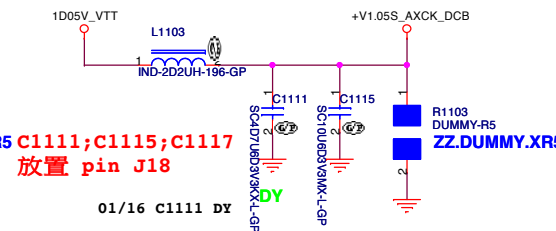


C1101 放置 pin V8
C1119 放置 pin K14

10/19 add RC1101 DY



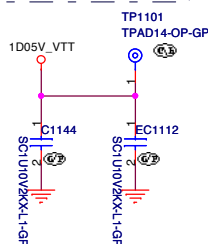
C1118;C1120;C1121
放置 pin A20



C1111;C1115;C1117
放置 pin J18

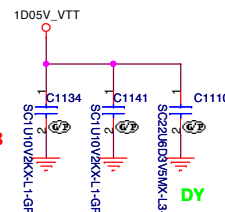
01/16 C1111 DY

C1144;C1112
放置 pin AE9

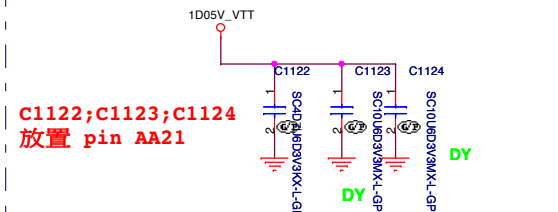


12/18 C1112 改為EC1112 FOR EMI, 1uF 上件

C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8



01/16 C1110 DY



C1122;C1123;C1124
放置 pin AA21

01/16 C1123 DY

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (Power CAP2)		
Size	Document Number	Rev
Custom	LT41	-1
Date:	Tuesday, January 20, 2015	Sheet 11 of 102



SSID = MEMORY

WWW.ALISALER.COM

BOM1

緯創資通		Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichia,		Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DDR3L-SODIMM2			
Size	Document Number	Rev	
A2	LT41	-1	
Date	Tuesday, January 20, 2015	Sheet	18 of 102

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
(Reserved) SODIMM SODIMM4		
Size	Document Number	Rev
A4	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 14 of 102

SSID = PCH

USB2.0 Table

Pair	Device
0	USB3.0 Port 1 (USB_OC#0)
1	USB3.0 Port 2 (with Debug Function) (USB_OC#1)
2	NC
3	Camera
4	USB2.0 Port 4 (USB_OC#2)
5	WLAN(Bluetooth)
6	NC
7	Panel Touch

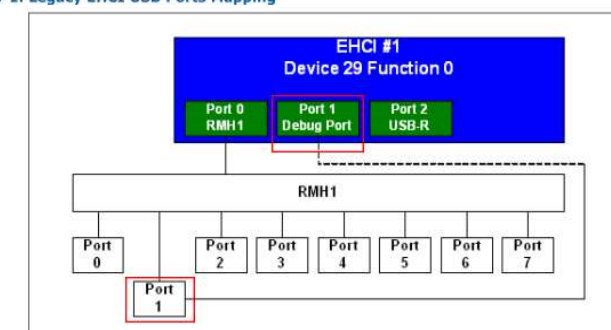
USB3.0 Table

Pair	Device
1	USB3.0 Charger Port 1
2	USB3.0 Port 2
3	Reserved
4	USB3.0 Card Reader Port 2

USB3.0 SKT1

USB3.0 SKT2

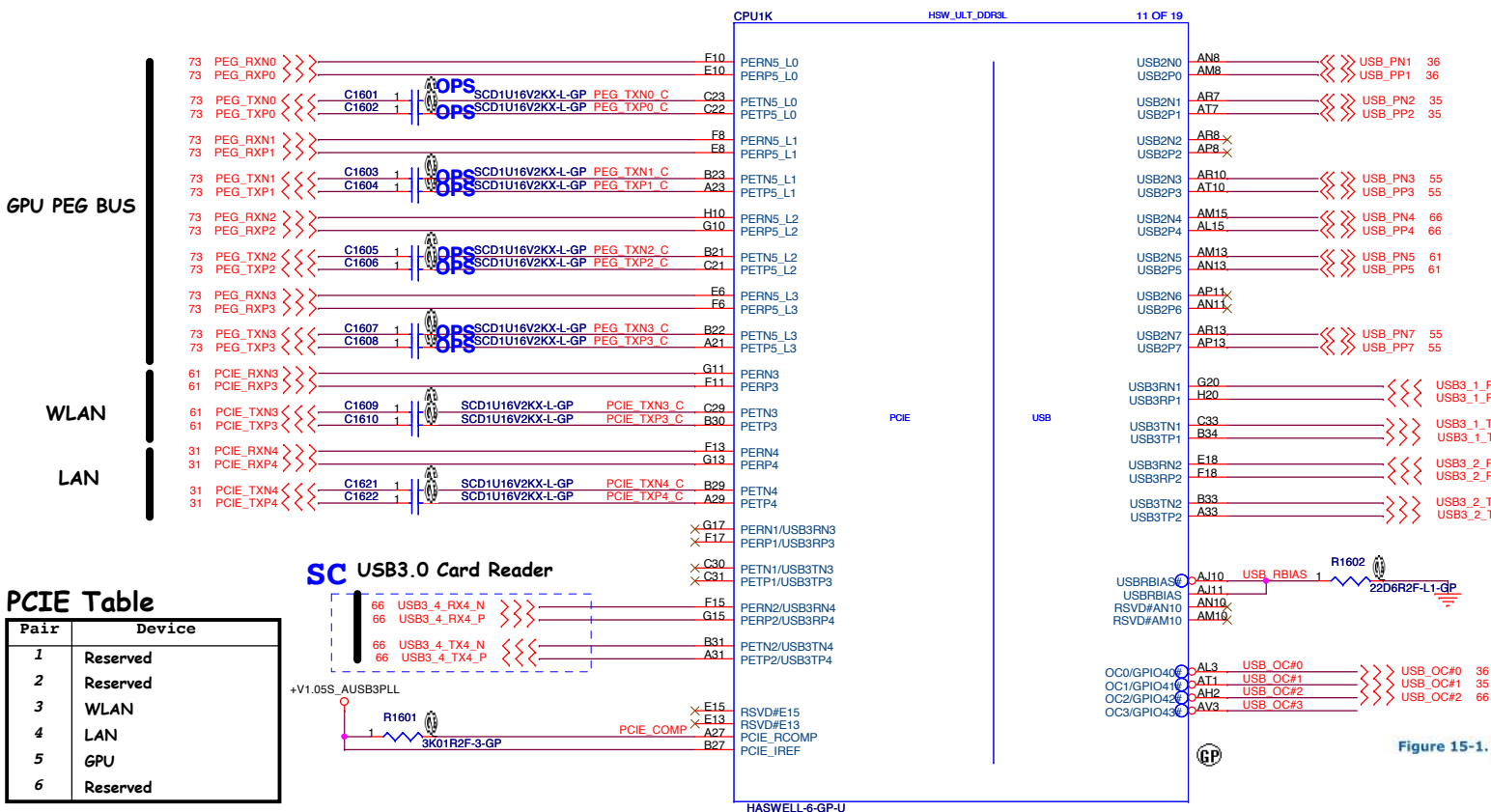
Figure 15-1. Legacy EHCI USB Ports Mapping



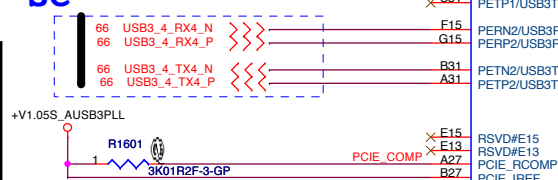
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title	CPU (PCI/USB)	
Size A3	Document Number	Rev
	LT41	-1
Date:	Tuesday, January 20, 2015	Sheet 16 of 102



SC USB3.0 Card Reader

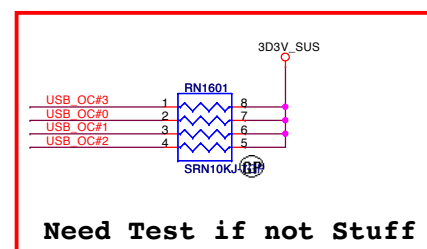


PCIe Table

Pair	Device
1	Reserved
2	Reserved
3	WLAN
4	LAN
5	GPU
6	Reserved

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

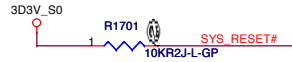
SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3



Need Test if not Stuff

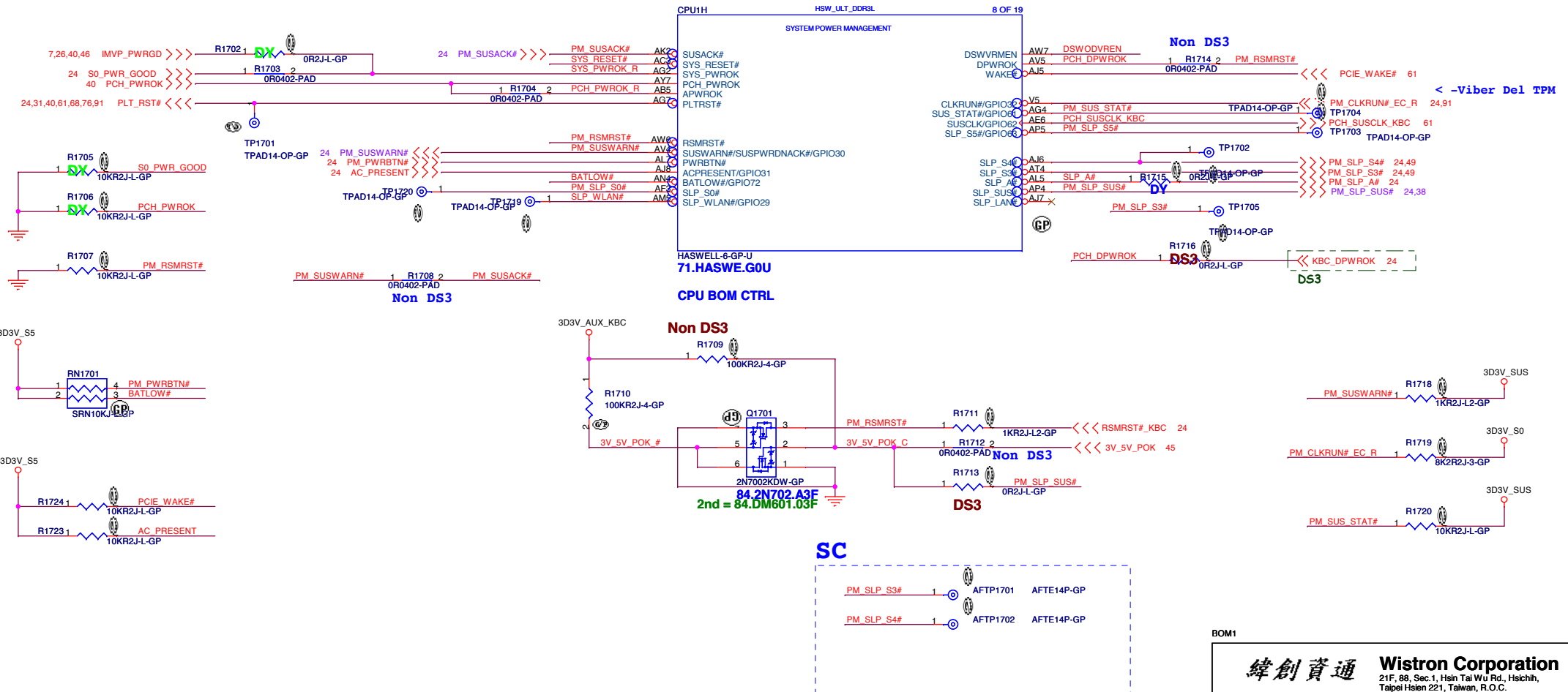
SSID = PCH

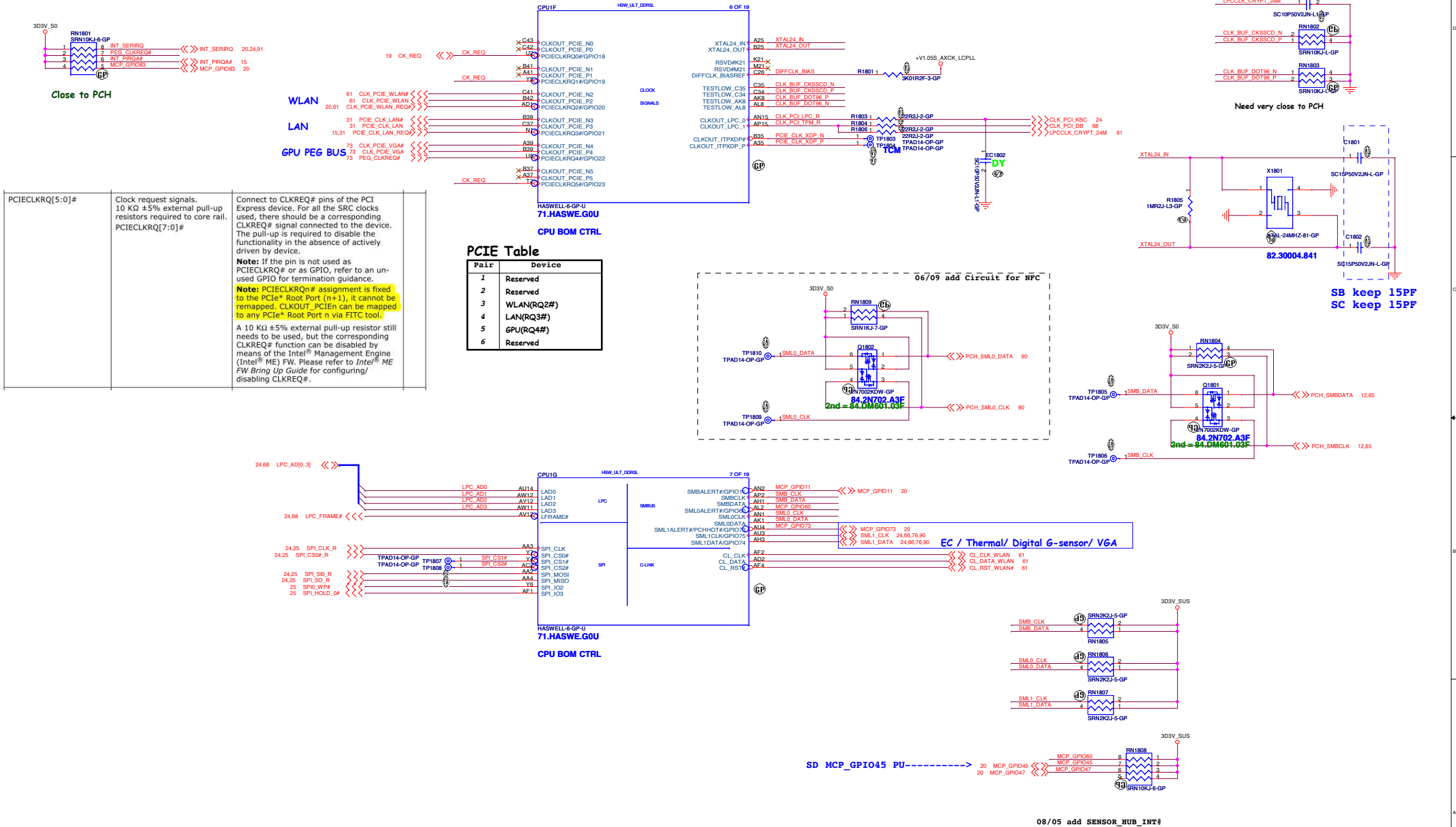
Follow Intel CRB



Bit	Description
31:3	Reserved
2	WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': <ul style="list-style-type: none">Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. NOTE: Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled





SSID = PCH

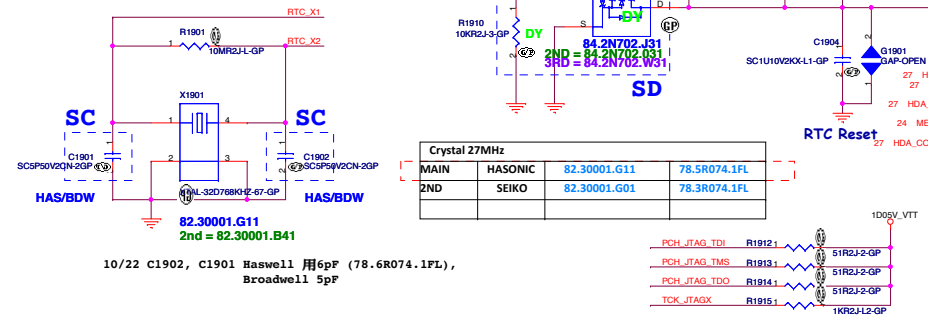
X1901 32D768KHZ BDW U SPEC:

32 Real Time Clock (RTC) Design Guidelines

Note: Unless otherwise indicated, this content pertains to **Broadwell-U, Broadwell-Y and Broadwell-E** 1-chip platforms. Information relating specifically to one platform only (Broadwell-U, Broadwell-Y or Broadwell-E) will be marked with "BDW-U", "BDW-Y" or "BDW-E" in paragraph margins as appropriate.

Note: **Has Crystal 32K ± 50ppm**

The PCH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.



Crystal 27MHz			
MAIN	HASONIC	82.30001.G11	78.5R074.1FL
2ND	SEIKO	82.30001.G01	78.3R074.1FL

10/22 C1902, C1901 Haswell 用6pF (78.6R074.1FL), Broadwell 5pF

Flash Descriptor Security Override	
HDA_SDOOUT	Low = Default High = Enable

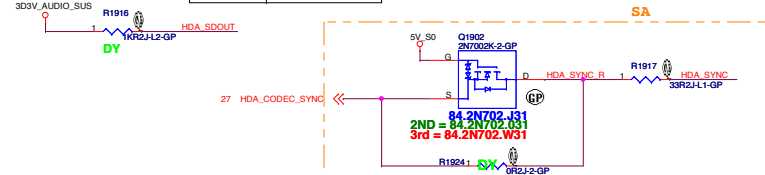


Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0	PCIe* Port 6 Lane 1	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3

2.1

PCIe SSD

PCIe SSD is one of the new features in Broadwell (2014) platform. In Haswell (2013) platform, only SATA-based SSD is supported. Moving SSD to PCIe gives better SSD performance over previous generation. M.2 Socket 2 supports both SATA and PCIe based SSDs. Figure below shows the configuration of High Speed I/Os in 2013/2014 PCH. The Haswell board can be made ready for both, **the optional PCIe SSD and SATA SSD**, by routing PCIe Port 6 Lane 0 and Lane 1 to the M.2 Socket 2 connector. For details on M.2 signals and pins for SATA and PCIe, please refer to Documentation Table below, M.2 row.

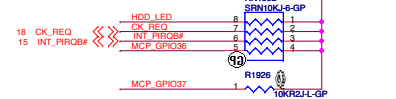
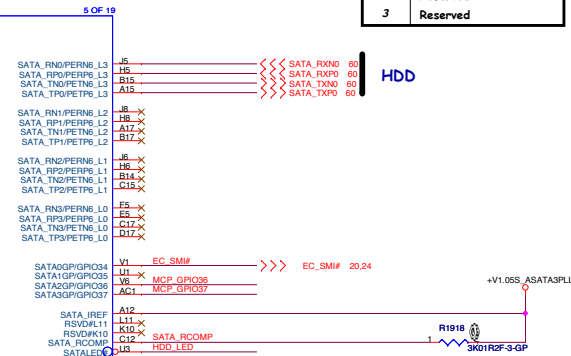
2-1. Configuration of High Speed I/Os in 2013/2014

USB3 P1	USB3 P2	USB3 P3	USB3 P4	PCIe P1	PCIe P2	PCIe P3	PCIe P4	PCIe P5	PCIe P6	PCIe P7	PCIe P8	PCIe P9	PCIe P10	PCIe P11	PCIe P12	PCIe P13	PCIe P14
Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14	Lane 15	Lane 16	Lane 17	Lane 18

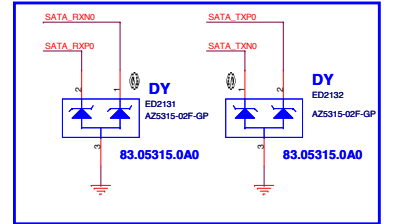
SATA Table

Pair	Device
0	HDD/SSD
1	NGFF SATA
2	Reserved
3	Reserved

HDD



EMC HDD TVS need to close CPU

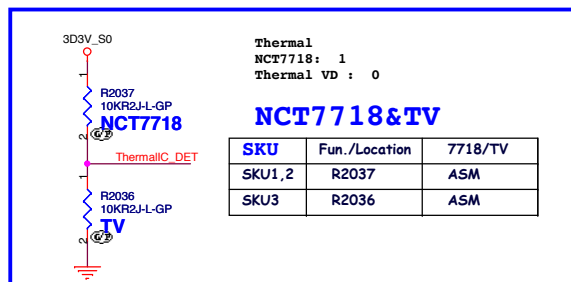


Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron BOM permission

偉創資通 Wistron Corporation	
21F, 8R, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 321, Taiwan, R.O.C.	
CPU (RTC/LPC/SATA/HDA)	
Size Custom	Document Number LT41
Date: Tuesday, January 20, 2015	Sheet 19 of 102

SSID = PCH

Thermal



SB

08/06 add SENSOR_HUB_INT#

08/14 add NFC Detect pin

08/05 add SENSOR_HUB_INT#

Default:Low

UMA&OPS

UMA&OPS

SKU	Fun./Location	UMA/DIS
SKU1	R2013	ASM
SKU2~5	R2014	ASM

CPU1J

HSW_ULT_DDR3L

10 OF 19

MCP_GPIO76 P10
MCP_GPIO8 AU2
MCP_GPIO12 AM7
MCP_GPIO15 AD6
TOUCH_RST Y1
MCP_GPIO24 AD5
NFC_DETECT T3
MCP_GPIO27 AD7
GPIO28 AD7
GPIO26 AN3

ThermalC_DET AG6
RTC_DET_KBC AP1
AL4
AT5
AK4
AB6

DGPU_PRST# U4
VIDEO_THERM_ALERT# V3
TOUCH_INT P3
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46

MCP_GPIO13 AT3
SENSOR_HUB_INT# AH4
mSATA_DTCT# AM4
MCP_GPIO45 AG5
MCP_DETECT AG3

UC_DETECT AM3
AM2
P2
C4
L2
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81

NFC_REQ
LAN_DIS#
N5
V2

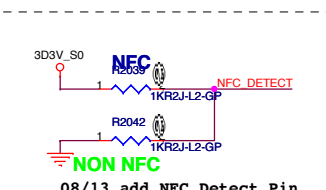
90 NFC_REQ <<< NFC REQ
LAN DIS#

27 HDA_SPKR <<< HDA SPKR

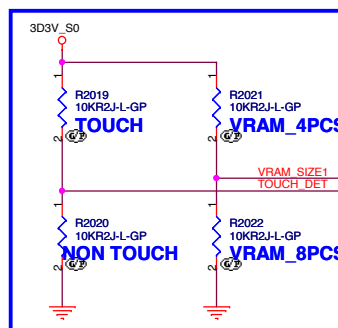
HASWELL-6-GP-UJ
71.HASWE.G0U

CPU BOM CTRL

6SPI0_MOSI_BB50_R(SSD_PWR)
PU RESERVED
PD SPI BUS



TOUCH&VRAM



VRAM SINGLE&DUAL

Fun./Location	SINGLE	DUAL
R2021	ASM	DY
R2022	DY	ASM

TOUCH

Fun./Location	TOUCH	NON TOUCH
R2019	ASM	DY
R2020	DY	ASM

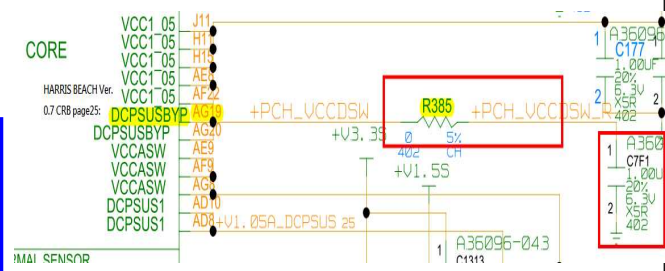
VRAM 900MHZ&1000MHZ

Fun./Location	900MHZ	1000MHZ
R2032	ASM	DY
R2033	DY	ASM

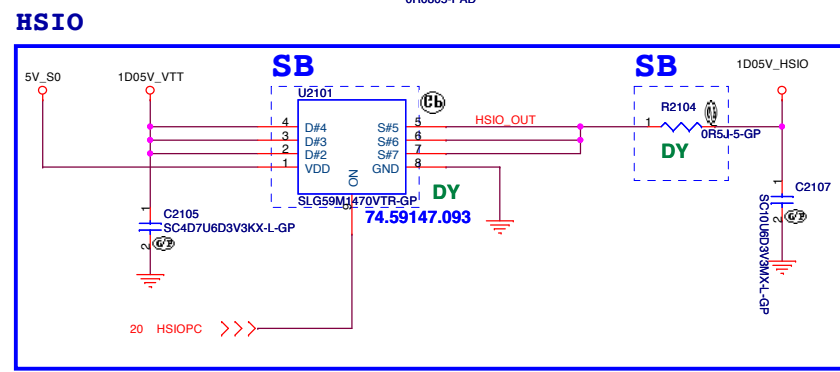
BOM1


緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CPU (GPIO/MISC)	
Size	Document Number
Custom	LT41
Date	Rev
Tuesday, January 20, 2015	-1
Sheet	102
20	

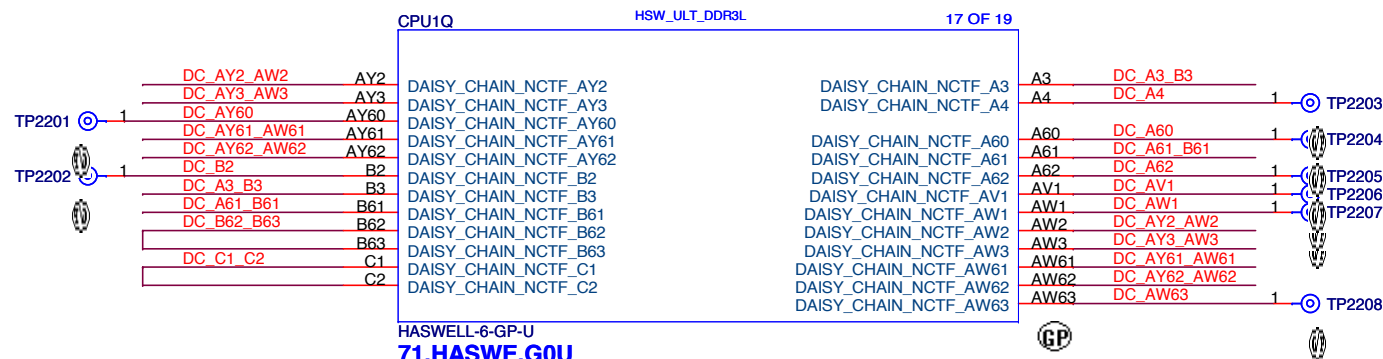
1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.](#)



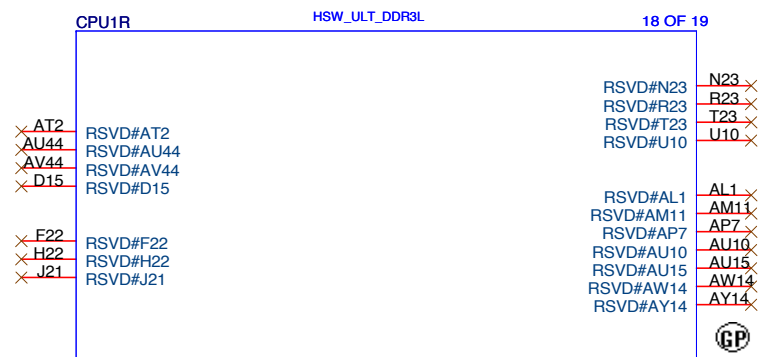
Function LOCATION	HSIO	NON HSIO
U2101	ASM	DY
R2104	ASM	DY
R2103	DY	ASM



BOM1			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (POWER1)			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet	21 of 102



CPU BOM CTRL

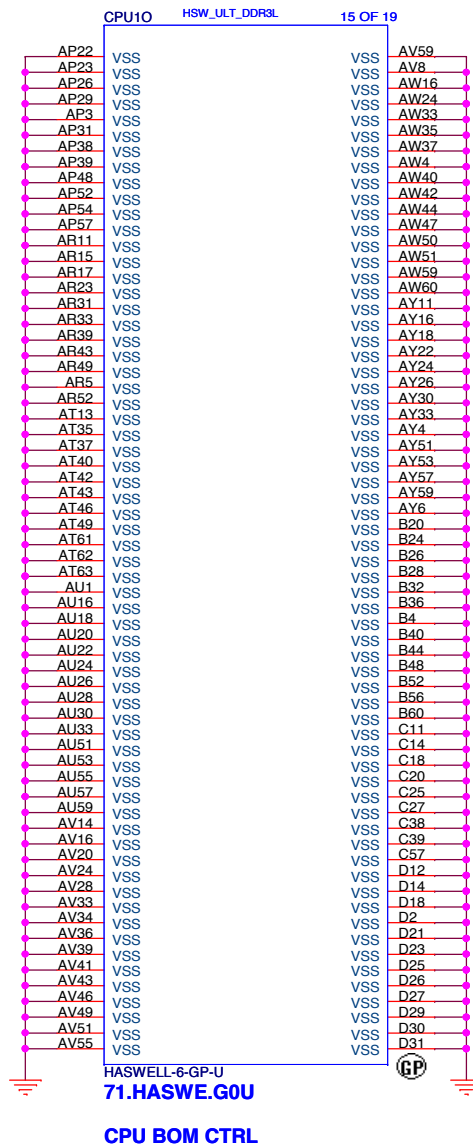
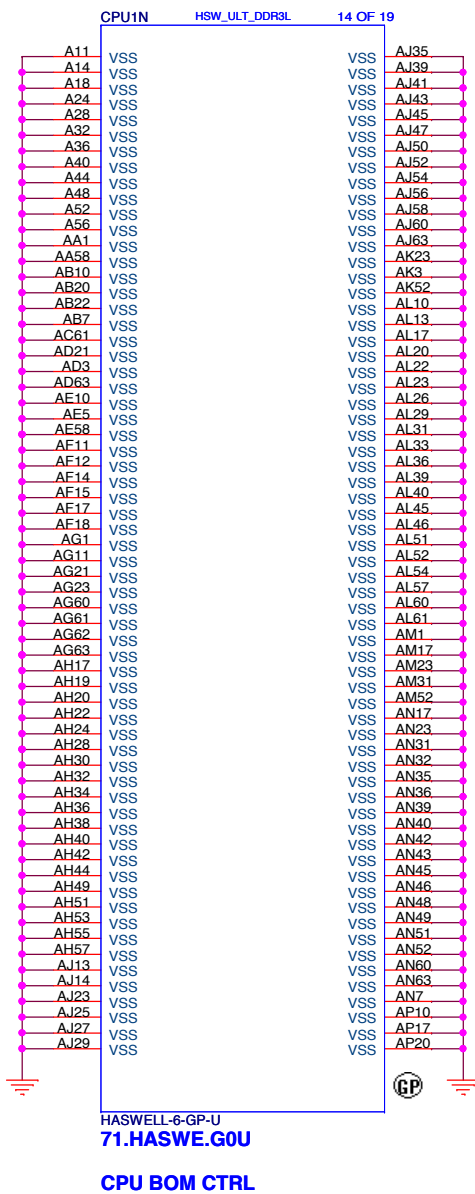


CPU BOM CTRL

BOM1

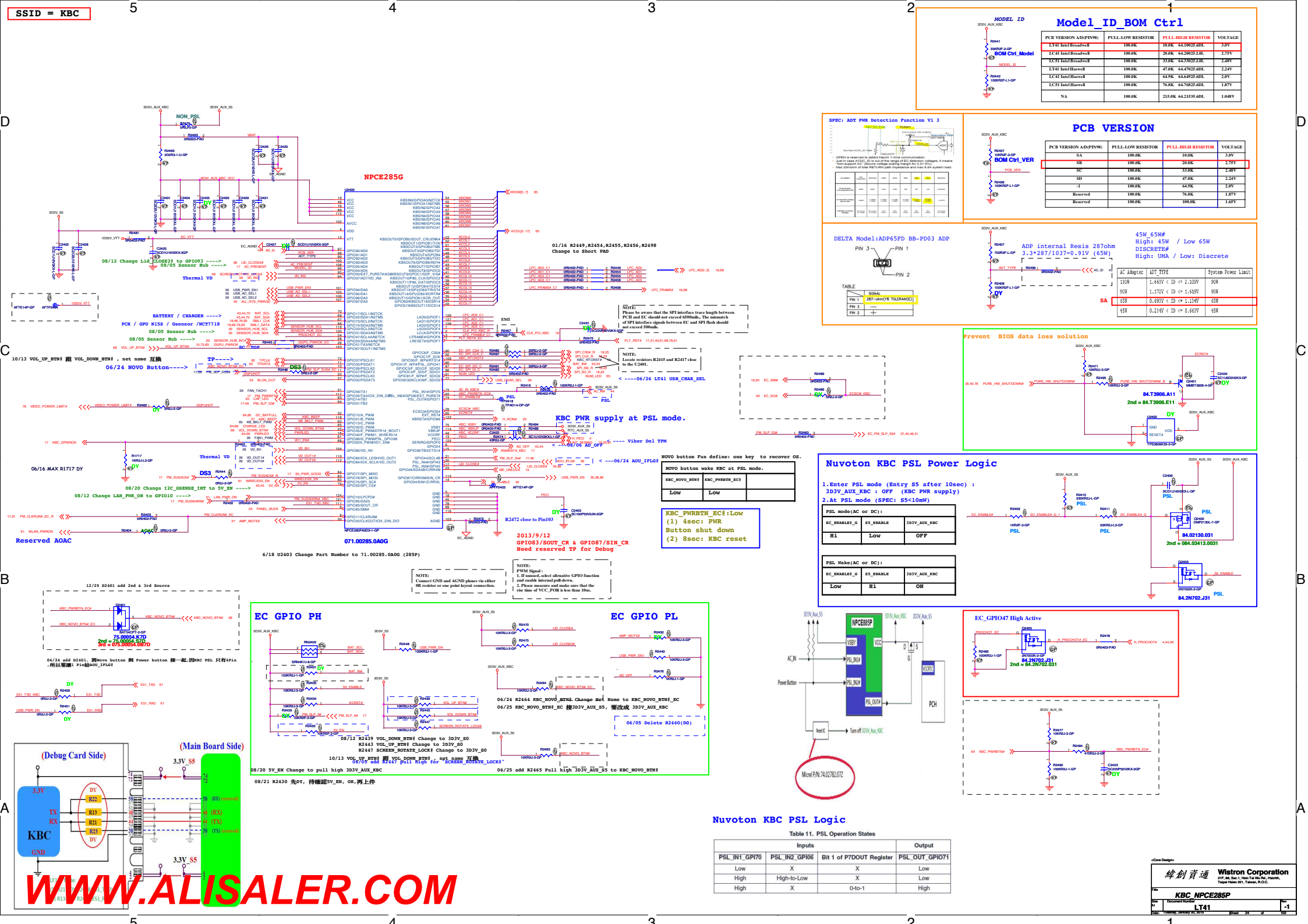
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (RSVD)			
Size	Document Number	Rev	
Custom	LT41	-1	
Date:	Tuesday, January 20, 2015	Sheet	22 of 102

SSID = PCH



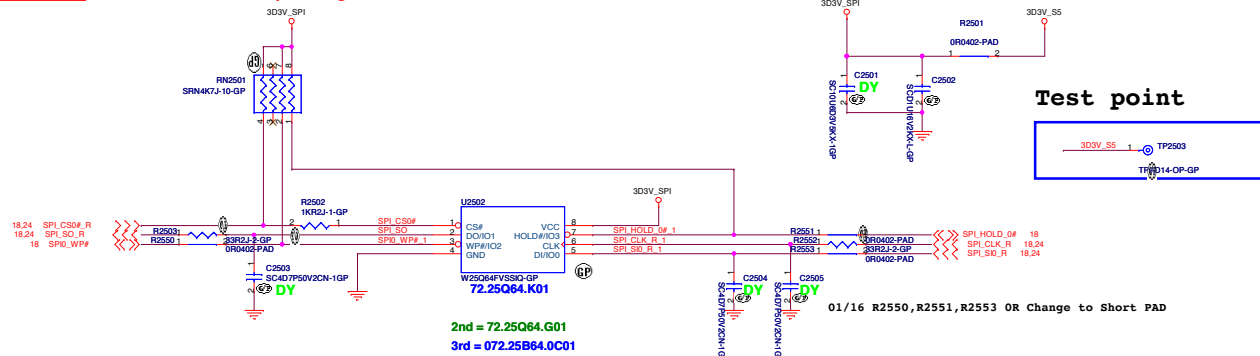
BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (VSS)			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 23 of 102



SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

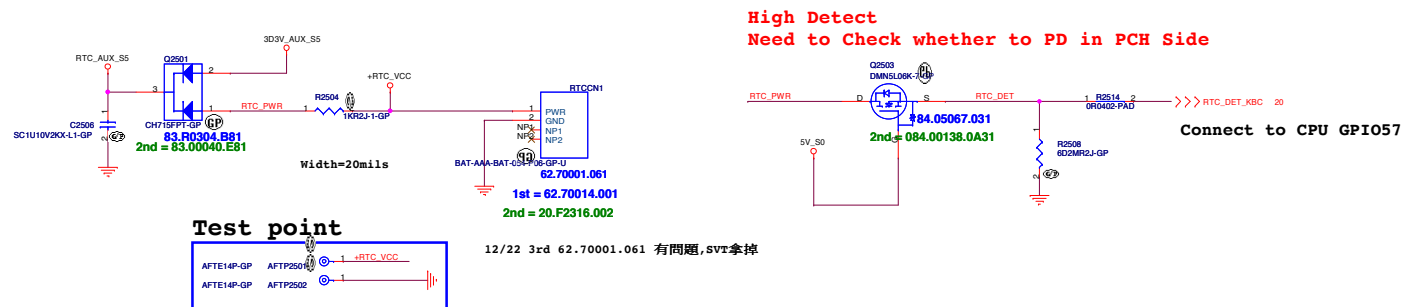


U2502			
Main	Winbond	W25Q64FV	72.25Q64.K01
SC	GIGADEVICE	GD25B64BSIGR	072.25B64.0001
SD	MICRON	N25Q64A13ESEC0F	72.25Q64.G01

Don't use MXIC 72.25647.00A

SSID = RBATT

SSID = RBATT



SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm rest

Close to Thermal sensor

3D3V_AUX_KBC

TBD

3D3V_AUX_KBC

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

TV

Note: Need R1717 PD: Enable Thermal VD Fun.
Note: (1) VD_IN1 for System sensor
(2) VD_IN2 for CPU sensor

Close to CPU chips

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

VD_IN1 24

VD_IN2 24

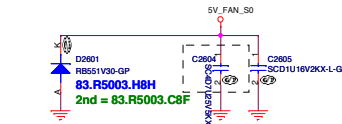
VD_IN1 24

VD_IN2 24

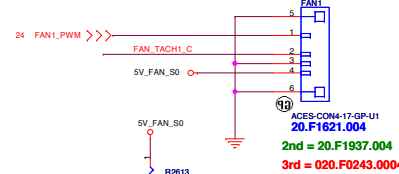
Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY

Layout 15 mil



07/31 C2604 Change part number 78.47523.5BL to 78.47522.L4L,
值为4.uF, 0805, 不同的是25V



83.R5003.H8H
2nd = 83.R5003.C8F

10/27 R2617 DY改上件

12/18 R2617 Change to Short PAD

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

83.00056.Q11
2nd = 75.00056.07D

ALERT# /T CRIT#
Pull-up Resistor

R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	87°C	97°C	107°C	117°C	
79°C	89°C	99°C	109°C	119°C	
81°C	91°C	101°C	111°C	121°C	
83°C	93°C	103°C	113°C	123°C	
85°C	95°C	105°C	115°C	125°C	

T_CRIT temperature strapping point



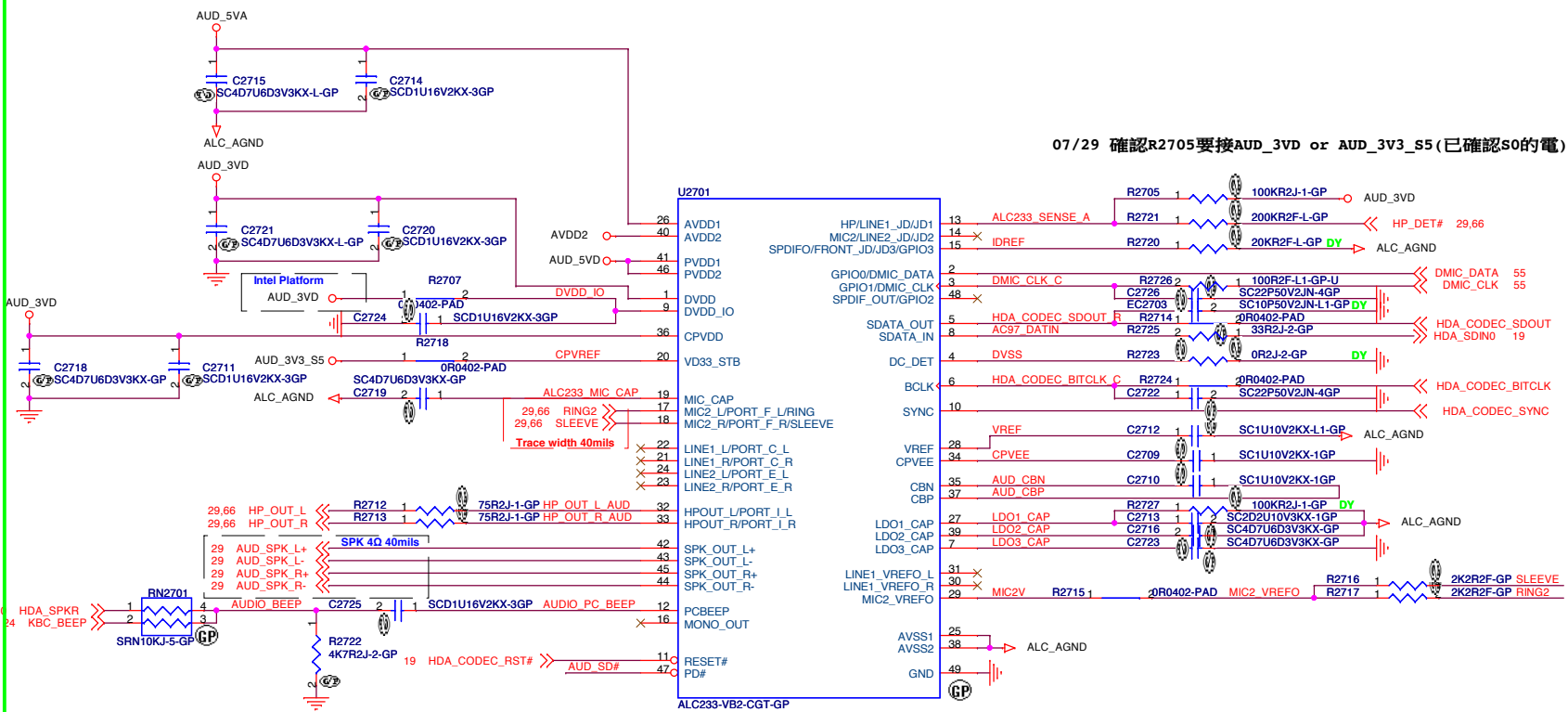
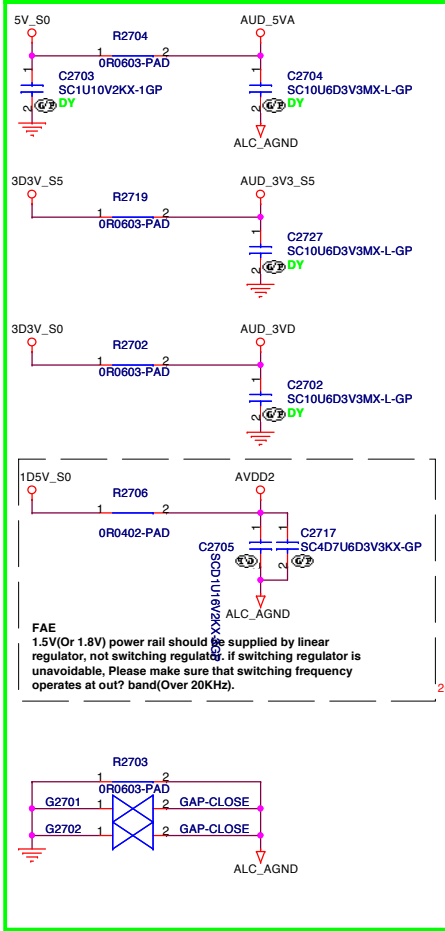
T8=85 degree

WWW.ALISALER.COM

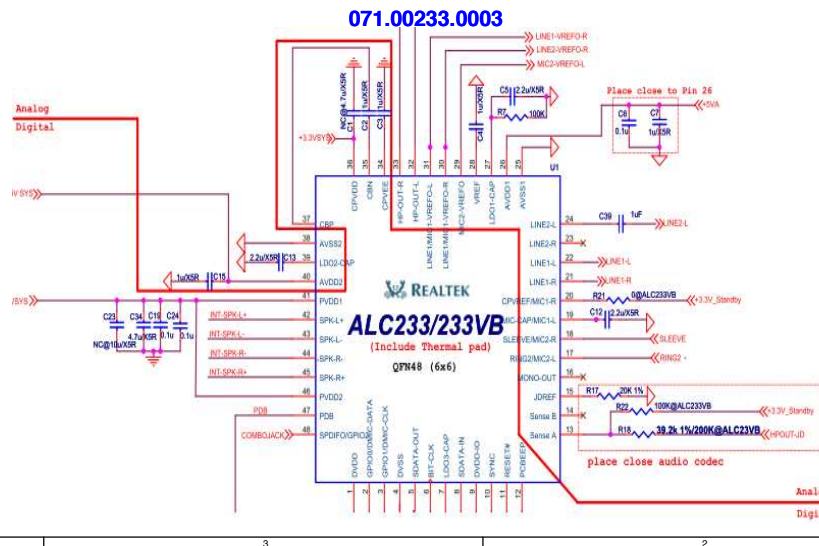
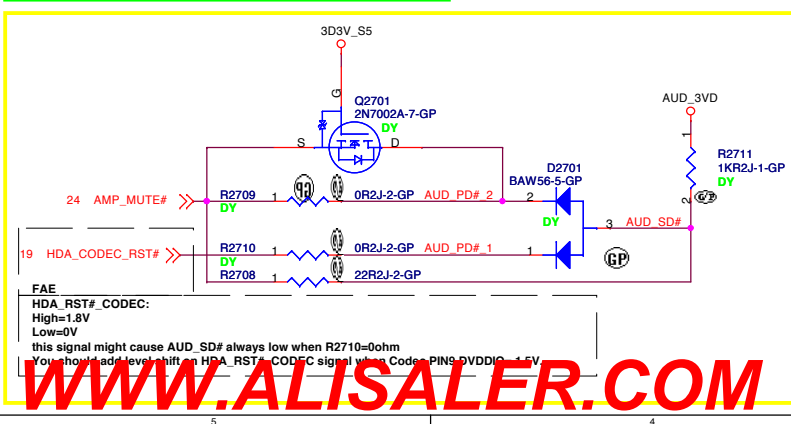
BOM1

緯創資通 Wistron Corporation
21F, 6B, Sec. 1, Hsin Tsu Wu Rd., Hsinchu,
Taippei Hsien 301, Taiwan, R.O.C.

File	Document Number	Rev
Thermal 7718/Fan Controller P2793	LT41	-1
Date: Tuesday, January 20, 2015	Sheet 26 of 102	



07/29 確認R2705要接AUD_3VD or AUD_3V3_S5(已確認S0的電)

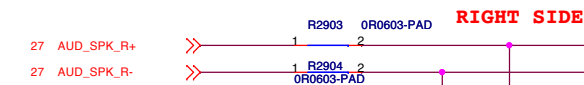


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
027 Audio Codec ALC233-VB2-CGT			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 27 of	102

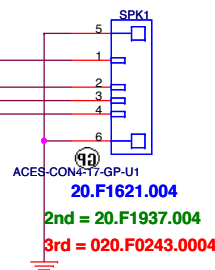
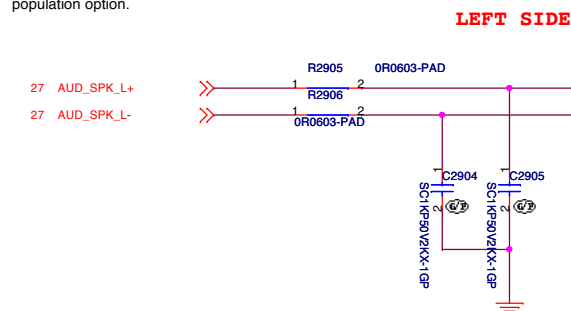
BOM1	
<div>緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
TitleAudio Codec ALC233(Reserved)	
SizeA2	Document NumberLT41
DateTuesday, January 20, 2015	Rev-1
Sheet 26 of 102	

INTERNAL STEREO SPEAKERS



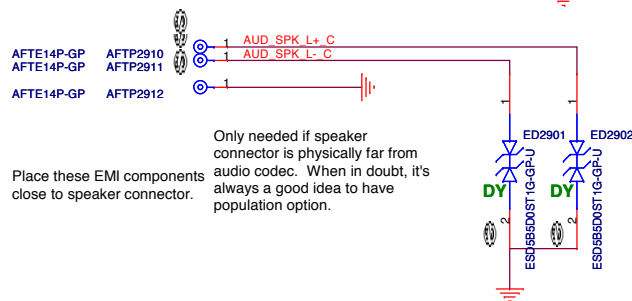
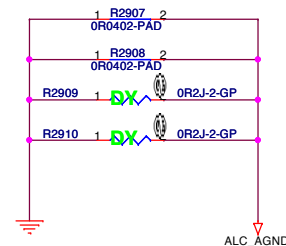
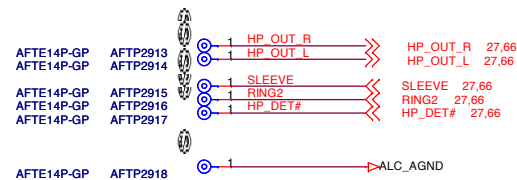
Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



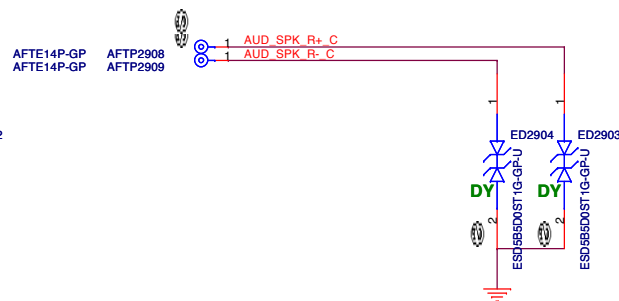
08/12 SPK1 20.F2348.007 Change to 20.F1621.004

06/12 SPK1 原本為4Pin, 換7 pin 接 Hall Sensor 訊號



Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



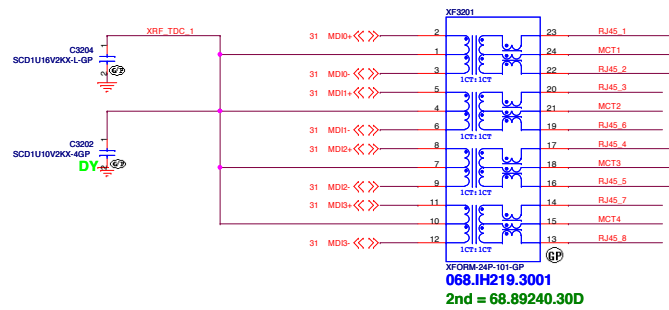
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			MIC/SPEAKER/AUDIO JACK	
Size	Custom	Document Number	LT41	Rev
Date:	Tuesday, January 20, 2015	Sheet	29	of 102
			-1	

5					4					3					2					1				
D																								
C																								
B																								
A																								
BOM1																								
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>																								
Title																								
Audio Jack_ (Reserved)																								
Size		Document Number																		Rev				
Custom		LT41																		-1				
Date:		Tuesday, January 20, 2015												Sheet		30		of		102				
5					4					3					2					1				

10/100M/1000M Lan Transformer

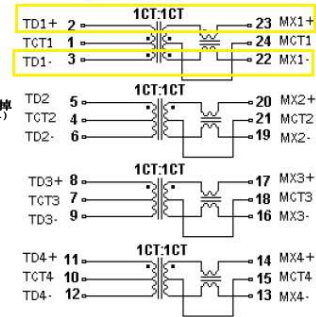


1000M Lan Transformer pin define

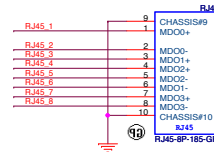
Part Number	Insertion Loss (dB Max) 1-100MHz	Return loss (dB MIN @100MHz)			
IH-106-A	-1.0	-18	-14.4	-13.1	

SCHEMATICS :

Pin Define



LAN Connector



022.10001.00A1

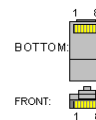
2nd = 022.10001.0571

08/13 RJ45 22.10019.141 Change to 022.10001.00A1

RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BL_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BL_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BL_DB+
4	Not connected or BiDirectional	n/c	n/c	BL_DC+
5	Not connected or BiDirectional	n/c	n/c	BL_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BL_DB-
7	Not connected or BiDirectional	n/c	n/c	BL_DD+
8	Not connected or BiDirectional	n/c	n/c	BL_DD-

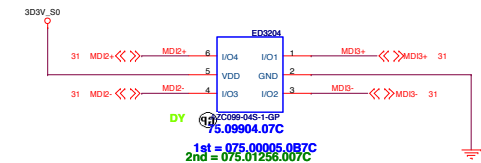
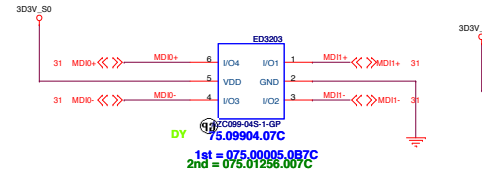
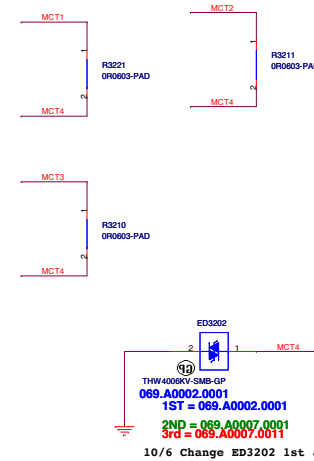
The connector is 8 pin RJ45 (8P8C) male



The associated connector is 8 pin RJ45 (8P8C) female



10/100/1000 LAN surge circuit For test stuff



8/25 將ED3203,ED3204 屬性ESD STUFF OPTION 改成DY, 上件會無法Wake on Lan

10/13 ED3203,ED3204 改成跟ED3501一樣, 增加三個Source

10/23 將3rd Source拿掉 75.09904.07C, 因為已有案子50米網線測不過(Part number跟ED3501一樣,BOM別帶錯)

10/23 ED3203, ED3204 ESD STUFF OPTION改 DY,不上件

AZ&NON AZ

Function LOCATION	AZ	NON AZ
ED3102	DY	ASM
R3114	DY	ASM
ED3103	ASM	DY
ED3104	ASM	DY
ED3105	ASM	DY
ED3106	ASM	DY
ED3107	ASM	DY
ED3108	ASM	DY
R3112	ASM	DY
R3115	ASM	DY
R3116	ASM	DY
R3117	ASM	DY
R3118	ASM	DY
R3119	ASM	DY
R3120	ASM	DY

06/13 Delete LAN_AGND

BOM1

緯創資通 Wistron Corporation
21F, 6F, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title LAN CONNECTOR		
Size A2	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 32	of 102

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>CARD Reader</div>		
Size <div>A4</div>	Document Number <div>LT41</div>	Rev <div>-1</div>
Date: Tuesday, January 20, 2015		Sheet 33 of 102

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB2.0 CONN

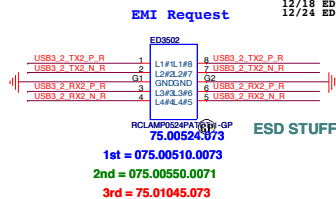
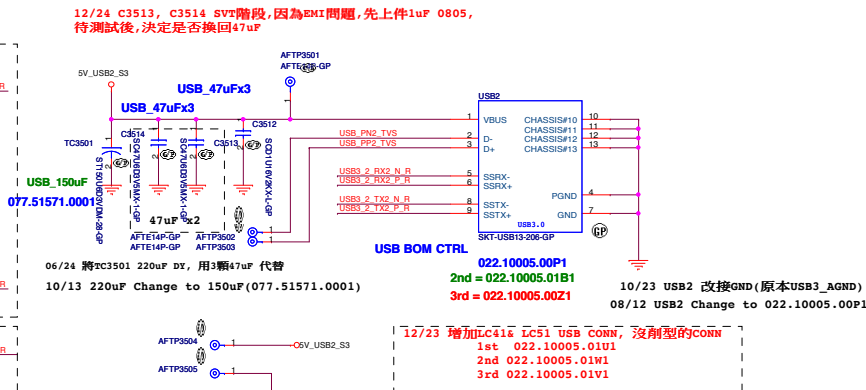
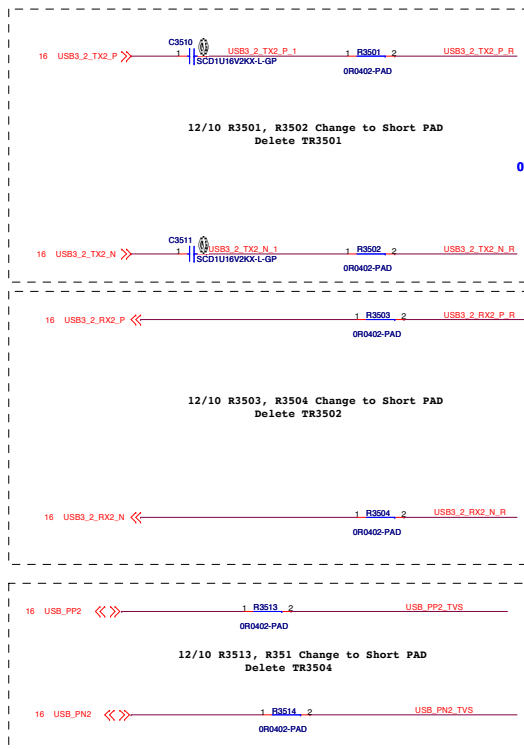
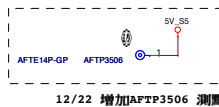
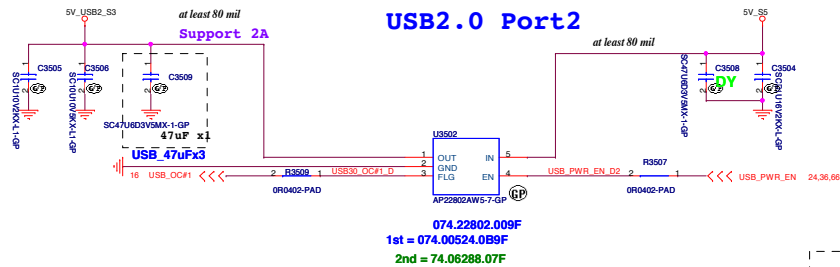
Size
A3

Document Number
LT41

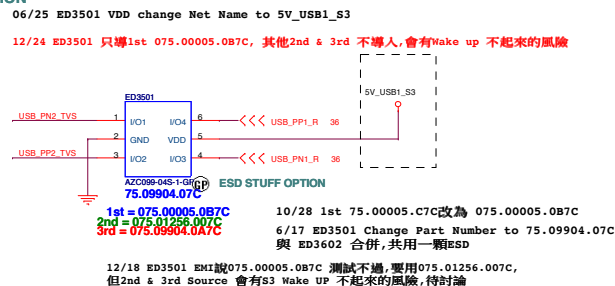
Date: Tuesday, January 20, 2015

Rev
-1

Sheet 34 of 102



ESD STUFF OPTION

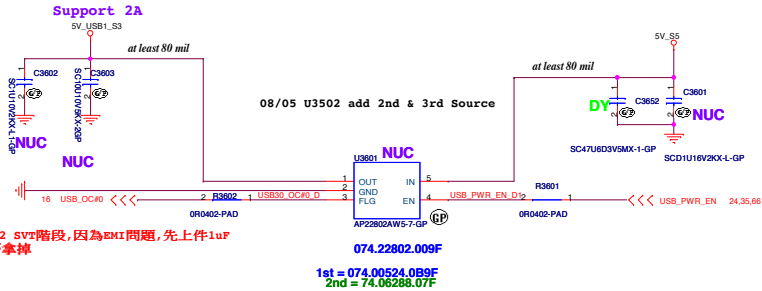


WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR

WWW.ALISALER.COM

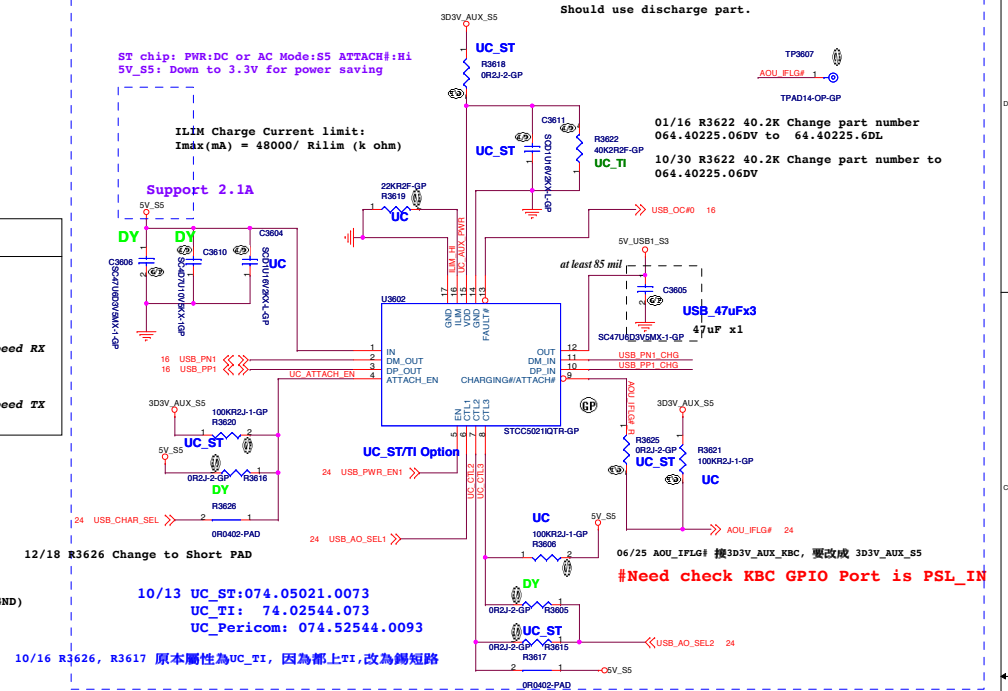
BOM1		緯創資通		Wistron Corporation	
				21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title					
USB3.0 CONN					
Size	Document Number			Rev	
A2	LT41			-1	
Date:	Tuesday, January 20, 2015		Sheet	36	of 102

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

USB charger



STCC5021 Truth Table

12/18 R3617 Change to Short PAD

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

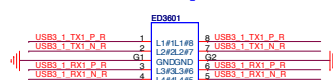
ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2544 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up	0	1	1	0	ILIM_HI
S3	S/P1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

Table 3 can be used as an aid to program the TPS2544 per system states however not restricted to below settings only.

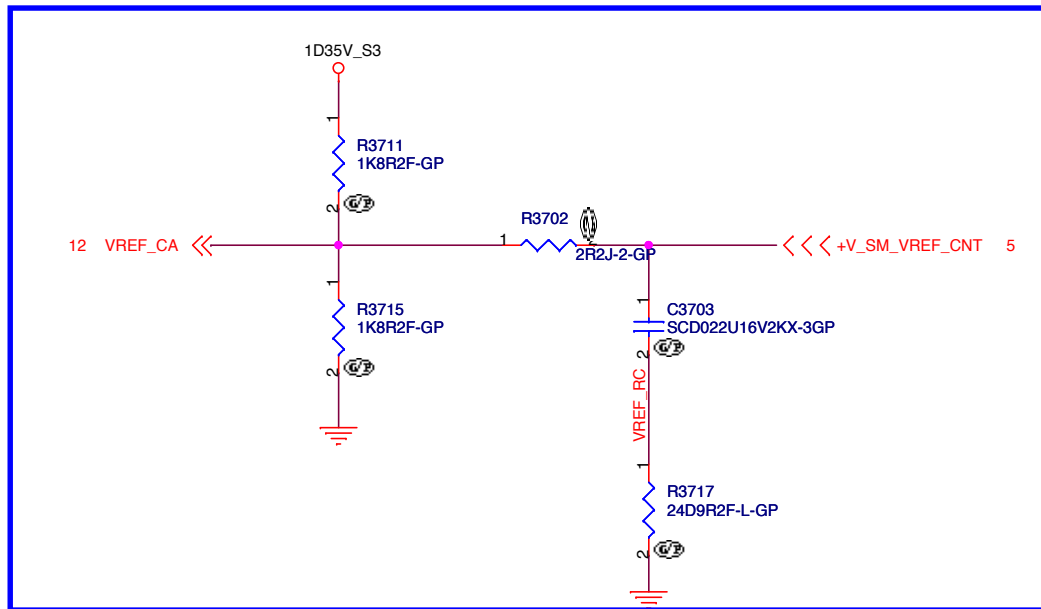
EMI Request



ESD STUFF OPTION

1st = 075.00590.0073
2nd = 075.00590.0073
3rd = 75.01045.073

EMI Request



For Intel Recommend Close to DIMM

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ADAPTER OCP / S3 reduction

Size
Custom

Document Number

LT41

Rev
-1

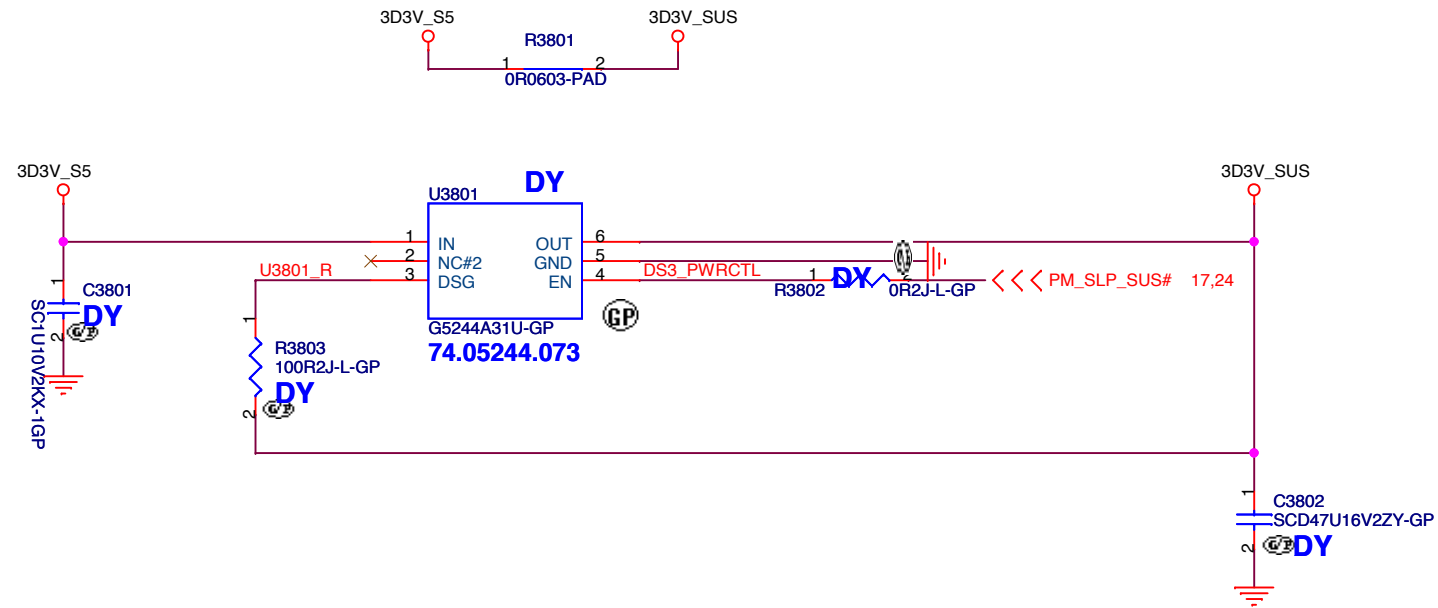
Date: Tuesday, January 20, 2015

Sheet 37 of 102

WWW.ALISALER.COM

DS3

Function LOCATION	DS3	NON DS3
R3801	DY	ASM
R1712	DY	ASM
R1709	DY	ASM
R1714	DY	ASM
C3802	ASM	DY
R1713	ASM	DY
R1716	ASM	DY
R2444	ASM	DY
R2446	ASM	DY
R2487	ASM	DY
R3802	ASM	DY
R3803	ASM	DY
U3801	ASM	DY
C3801	ASM	DY



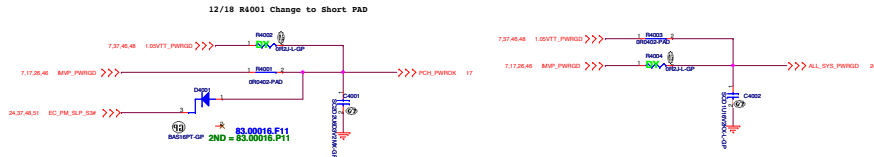
BOM1

緯創資通

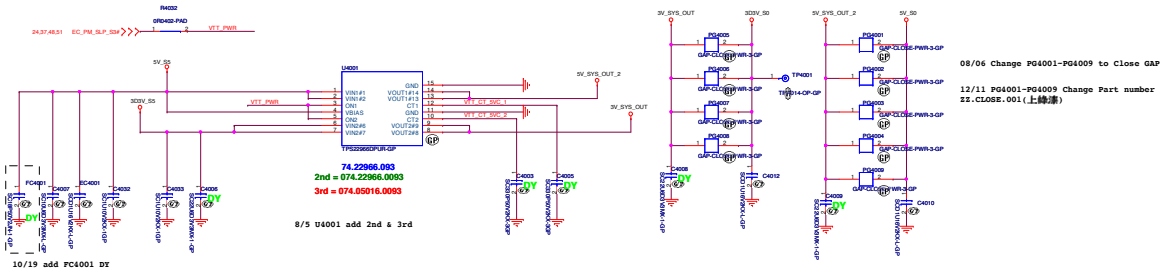
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D05 M		
Size	Document Number	Rev
Custom	LT41	-1
Date	Tuesday, January 20, 2015	Sheet 39 of 102

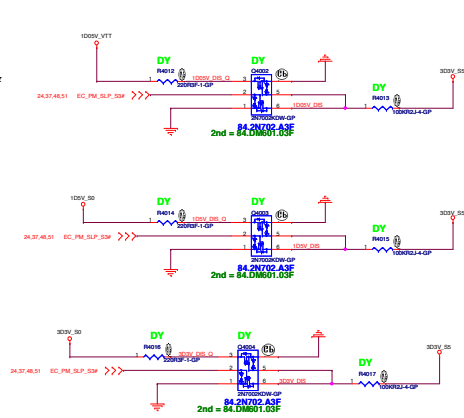
Power Sequence



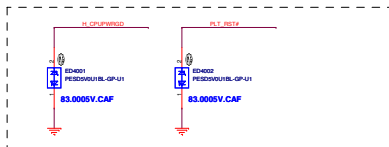
Run Power



Discharge circuit



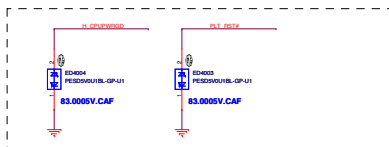
10/17 Delete 放電線路



10/16 add ED4001, ED4002

10/27 EMI上錯料, (083.00105.00AF)才是對的, 先把原來的DY

12/18 ED4001, ED4002 change Part Number to 83.0005V.CAF



12/18 add ED4003, ED4004 83.0005V.CAF

5

4

3

2

1

D

D

C

C

B

B

A

A

WWW.ALISALER.COM

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby1			
Size	Document Number		Rev
A	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet	41 of 102

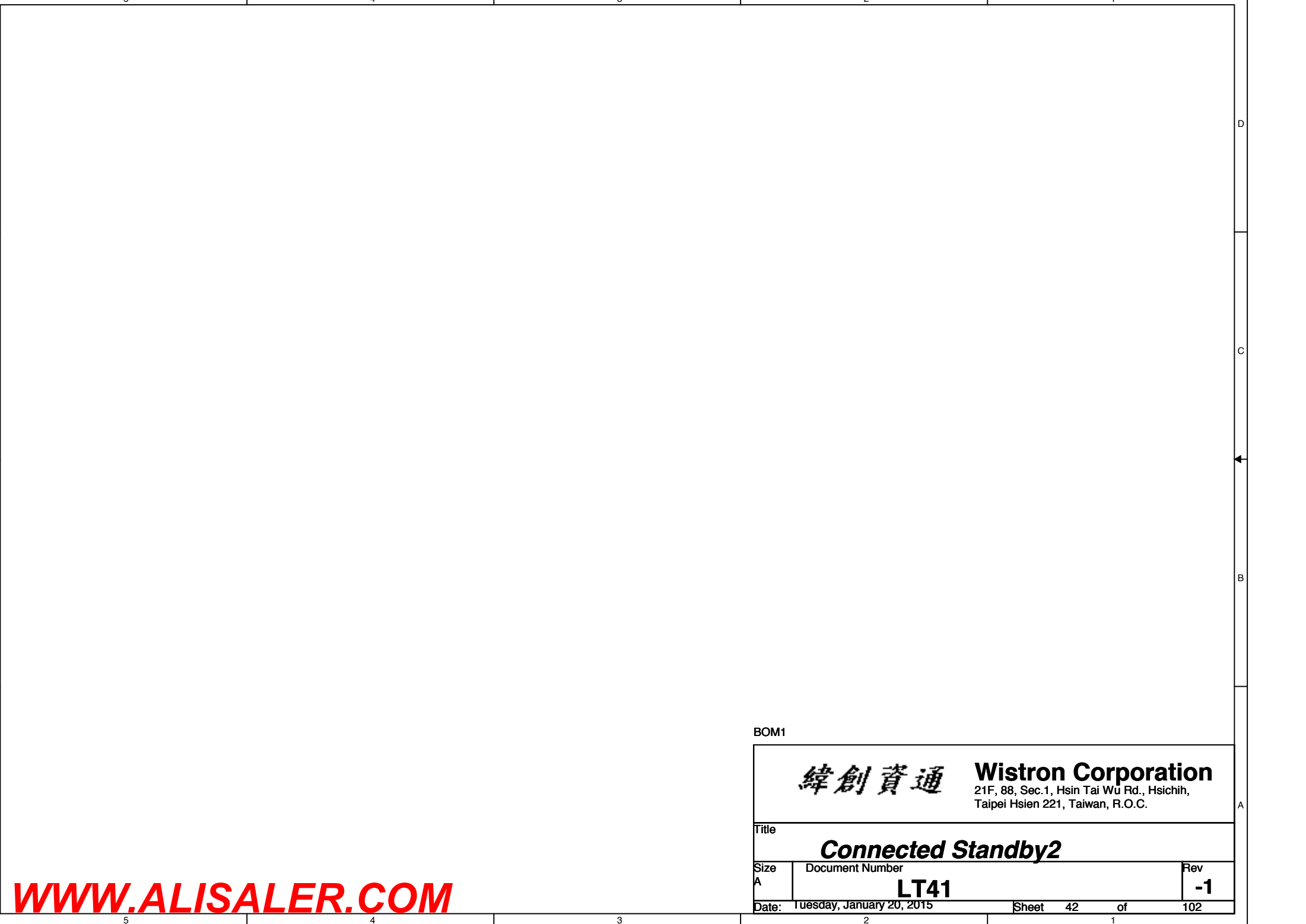
5

4

3

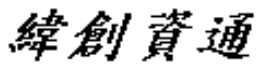
2

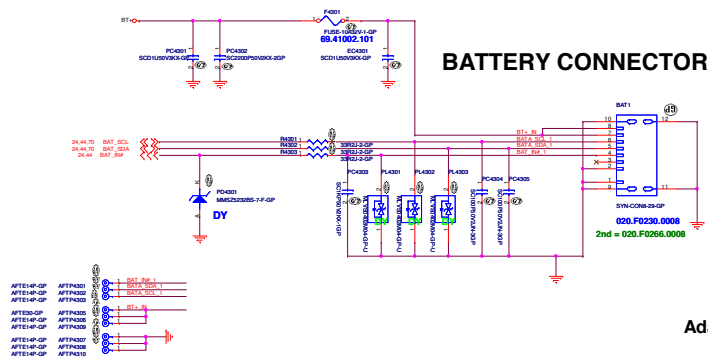
1



WWW.ALISALER.COM

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Connected Standby2			
Size A	Document Number LT41		Rev -1
Date: Tuesday, January 20, 2015	Sheet	42	of 102



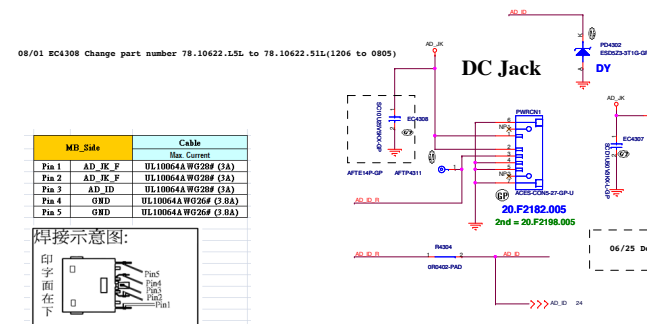
BATTERY CONNECTOR

Connector Pin Alignment(Vendor: Suyin,Aces)

Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

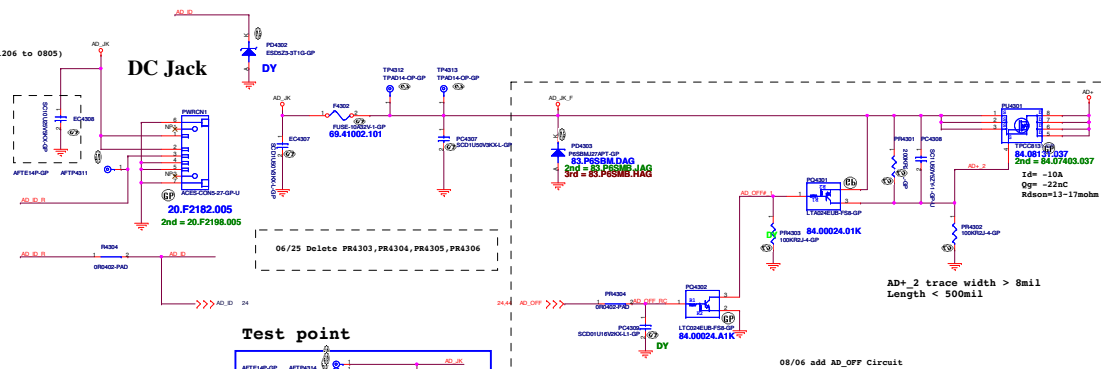
Adaptor in to generate DCBATOUT



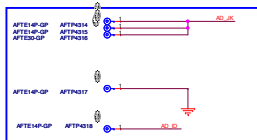
MB_Side		Cable
		Max. Current
Pin 1	AD JK F	UL10064A WG28# (3A)
Pin 2	AD JK F	UL10064A WG28# (3A)
Pin 3	AD ID	UL10064A WG28# (3A)
Pin 4	GND	UL10064A WG26# (3.8A)
Pin 5	GND	UL10064A WG26# (3.8A)

焊接示意图:

印字面在下

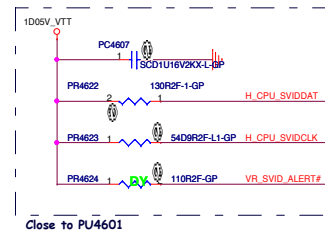


Test point



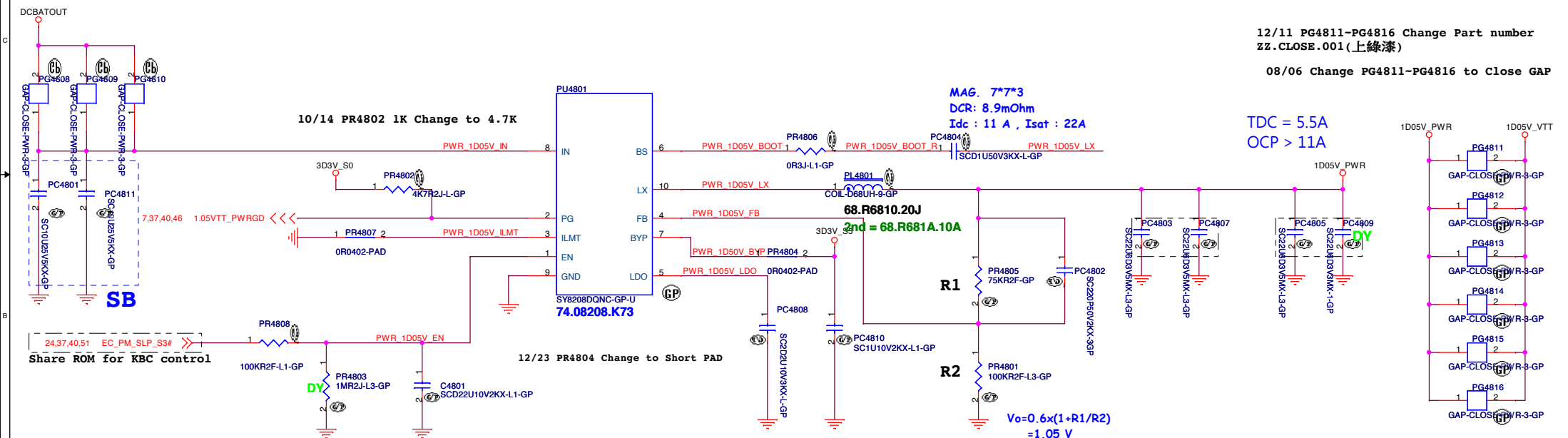
 緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.					
File					
DCIN JACK & BATT Conn					
Date	Document Number				New
R1	LT41				-
Value	UNSPECIFIED	UNITARY	Alt.	Model	Alt.

WWW.ALISALER.COM



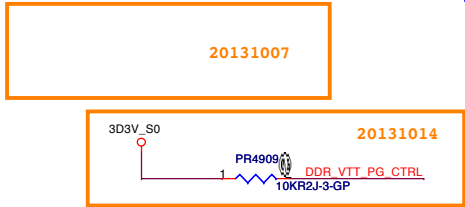
Title			
TPS51624 CPUCORE(1/2)			
Size C	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 46 of	102

SY8208D for 1D05V



WWW.ALISALER.COM

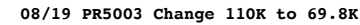
WWW.ALISALER.COM



STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

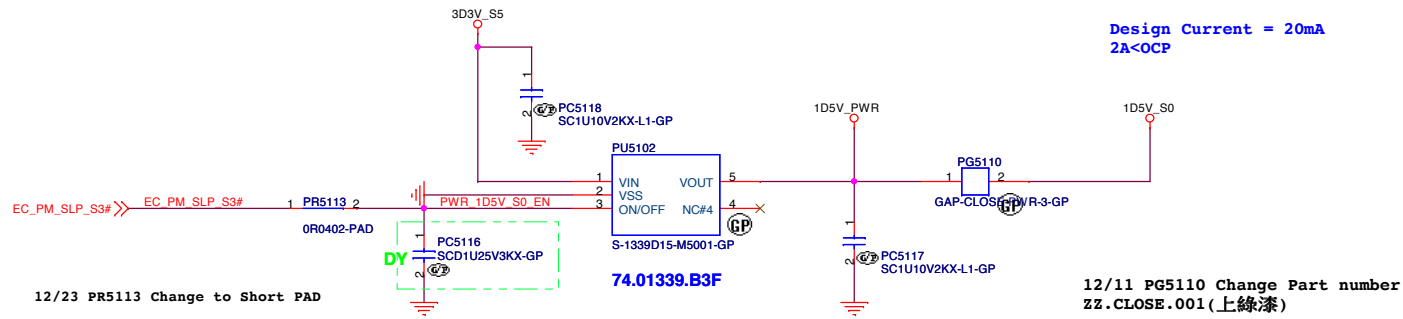
<div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div>			
Title			
TPS51716(VDDQ VTT)			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 49 of	102

08/12 Pin-8 of Pu5001 connect to net "15V PWR"



Sheet 50 of 102

RT9198 for 1D5V_S0



10/28 74.09198.B7F(鎖料) 改 74.01339.B3F

WWW.ALISALER.COM

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

No.	Title	Author	Date	Page
1	The first part of the book	John Doe	1998	100
2	The second part of the book	John Doe	1998	100
3	The third part of the book	John Doe	1998	100
4	The fourth part of the book	John Doe	1998	100
5	The fifth part of the book	John Doe	1998	100
6	The sixth part of the book	John Doe	1998	100
7	The seventh part of the book	John Doe	1998	100
8	The eighth part of the book	John Doe	1998	100
9	The ninth part of the book	John Doe	1998	100
10	The tenth part of the book	John Doe	1998	100

1D5V_S0 RT9198

Size
A3

Document Number

LT41Rev
-1

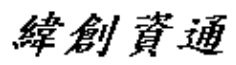
-1

Date: Tuesday, January 20, 2015

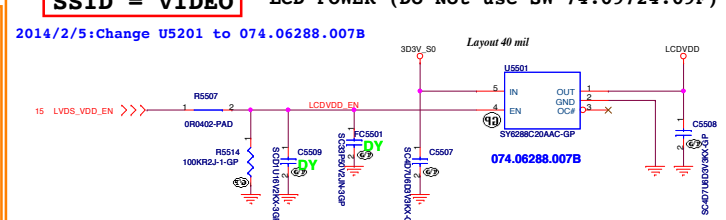
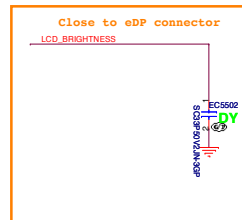
Sheet 51 of 102

BOM1	
<div>緯創資通Wistron Corporation 21F, 88, Sec-1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
CRT Board Connector	
Size Custom	Document Number LT41
Rev -1	
Date: Tuesday, January 20, 2015	
Sheet 53 of 102	

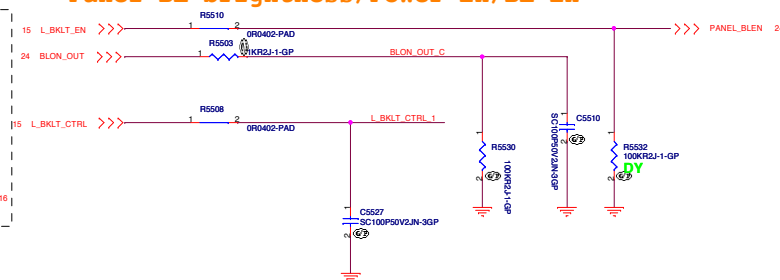
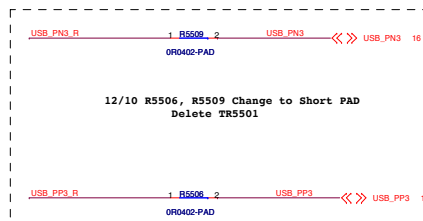
BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015		Sheet 54 of 102

LCD POWER (Do Not use SW 74.09724.09F)



Panel BL brightness/Power En/BL En



eDP Device

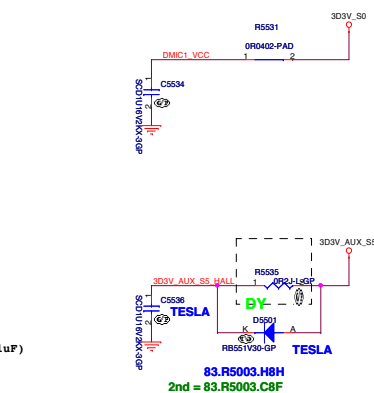
Item	Device
1	Lid
2	
3	DMIC
4	Panel Touch
5	Camera
6	eDP Panel



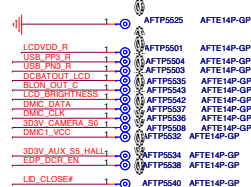
Touch control BD

mera

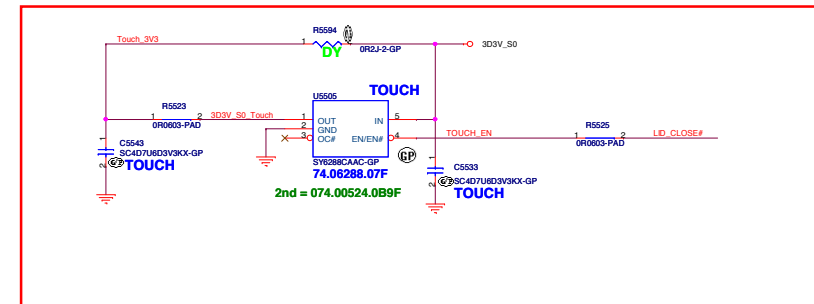
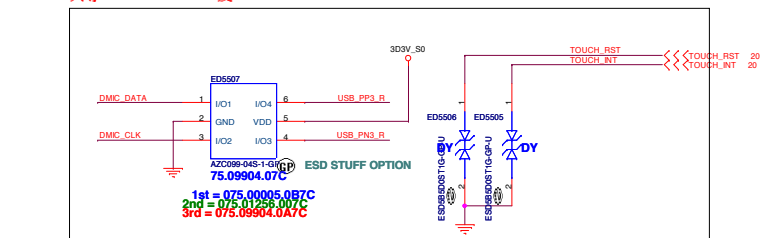
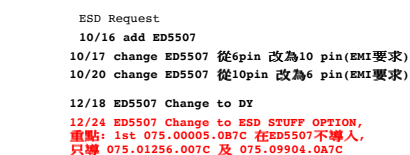
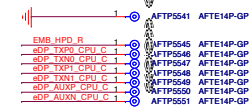
eDP Panel



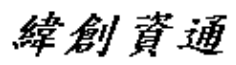
Test point



10/20 AFTP5503, AFTP5504 USB_PN3, USB_PP3 change to USB_PN3_R, USB_PP3_R



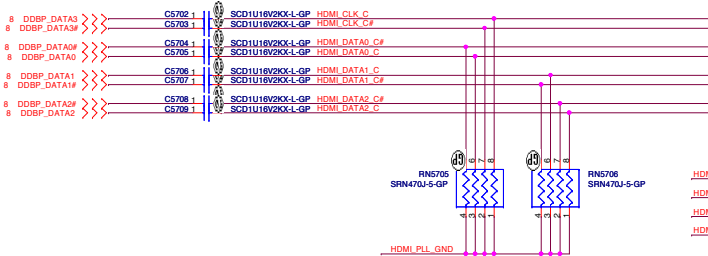
BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LT41		Rev -1
Date: Tuesday, January 20, 2015		Sheet 56 of	102

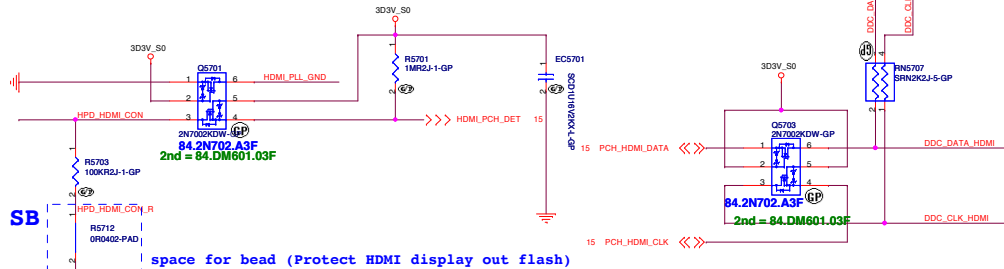
SSID = VIDEO

HDMI Passive Level Shifter

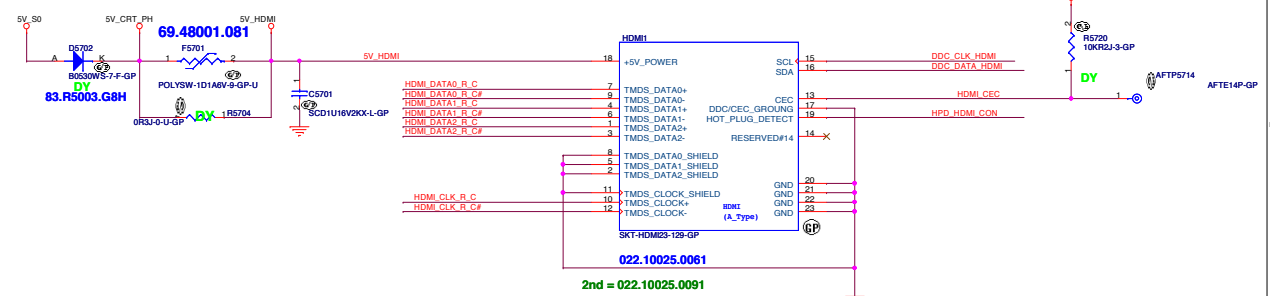
Close to HDMI Connector



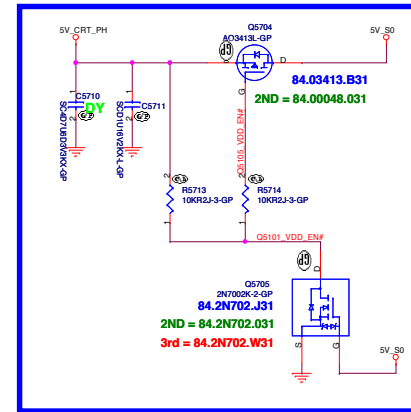
HDMI DDC Passive Level Shifter



HDMI CONNECTOR



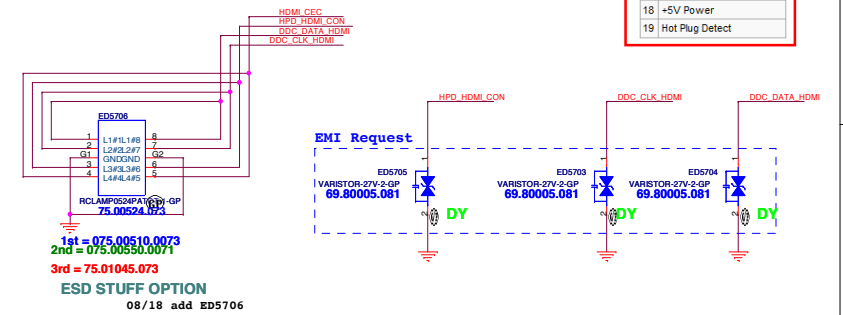
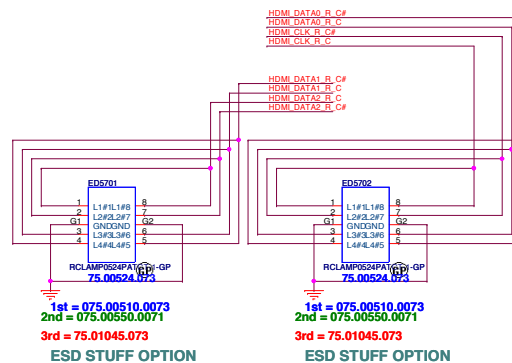
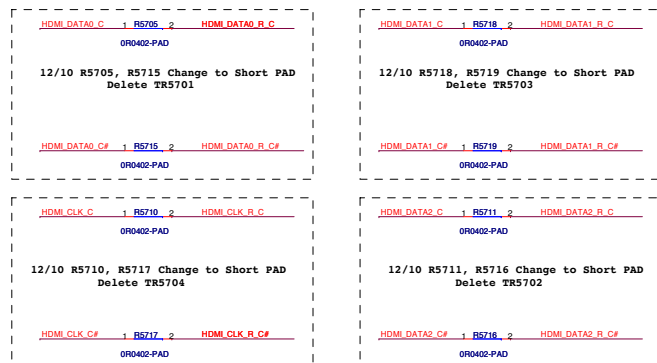
08/12 HDMI1 22.10296.B41 Change to 022.10025.0061



07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31

HDMI A type pin define
(Total: 19pin)

Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect



10/15 ED5701,ED5702,ED5706 Change Part number to 75.00524.073
12/18 ED5701,ED5702,ED5706 Change to DY
12/24 ED5701,ED5702,ED5706 Change to ESD STUFF OPTION

WWW.ALISALER.COM

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LT41</div>	Rev <div>-1</div>
Date: Tuesday, January 20, 2015		Sheet 58 of 102

SSID = Wireless

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NGFF SATA			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 59 of	102

SSID = SATA



WWW.ALISALER.COM

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD / NGFF SSD			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 60 of	102

Rev	-1
-----	----

(Blanking)

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
LT41

Date: Tuesday, January 20, 2015

Rev
-1

Sheet 63 of 102

The diagram shows the internal circuitry of the Tesla Powerwall 2 battery pack. It features a KBC_PWRBTN# 24 pin on the left, which is connected to a series of components including a diode (L6405 MLV50402M04-GP-U), a resistor (G6402), and a diode (G6403). The circuit is labeled with 'TESLA' and 'FLEX'. The output of the circuit is connected to the AFT14P-GP pin on the right. The diagram also shows a connection to the KBC_PWRBTN# 24 pin on the right, which is connected to a series of components including a diode (L6405 MLV50402M04-GP-U), a resistor (G6402), and a diode (G6403). The circuit is labeled with 'TESLA' and 'FLEX'. The output of the circuit is connected to the AFT14P-GP pin on the right. The diagram also shows a connection to the KBC_PWRBTN# 24 pin on the right, which is connected to a series of components including a diode (L6405 MLV50402M04-GP-U), a resistor (G6402), and a diode (G6403). The circuit is labeled with 'TESLA' and 'FLEX'. The output of the circuit is connected to the AFT14P-GP pin on the right.

24 KBC_PWRBTN# <<<

R6417 100R2J-2-GP

FLEX

C5402 0.5402 50V2KX-1GP

FLEX

C5401 62.40012.041

SW-TACT-72-GP-U3 PWRSH1

08/14 PWRSH1 Change to PWRSH1

10/14 PWRSH1 (Pin1,Pin3)KBC_PWRBTN#_R3 SWAP (PIN2,PIN4)GND

Electro-Optical Characteristics ($T_a=25^{\circ}\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V_F	1.7	---	2.3	V	$I_F=5\text{mA}$

84.2N702.J31

WHITE

2N7002K-2-GP

5V_SS

R6413

910R2J-1-GP

PB-LED_PWR_1

A

LED1

PB-LED_PWR_2

D

LED-W-42-GP

U6402

PWRLED

PWRLED 24.66

TESLA

83.19213.H70

TESLA

1st = 84.2N702.J31

2nd = 84.2N702.W31

10/14 R6413 510R Change to 910R

Symbol	Bin Code	Min.	Max.	Unit	Condition
I _v	P1	4.5	5.7	med	I _f =5mA
	P2	5.7	7.2		
	Q1	7.2	9.0		
	Q2	9.0	11.2		
	28	2.60	2.70		
V _f	29	2.70	2.80	V	I _f =5mA
	30	2.80	2.90		
	31	2.90	3.00		

Part No.	Chip		Lens Color
	Material	Emitted Color	
48-213/T3D-AP1Q2TY/3C	InGaN	Pure White	Yellow Diffused

[illegible]

AFTE14P-GP AFTP6410

AFTE14P-GP AFTP6409

1KBC PWRBTN# R

5V AUX SS

DC-BATFILL CHARGE LED

5V SS

PWRLED

AFTE14P-GP AFTP6401

AFTE14P-GP AFTP6402

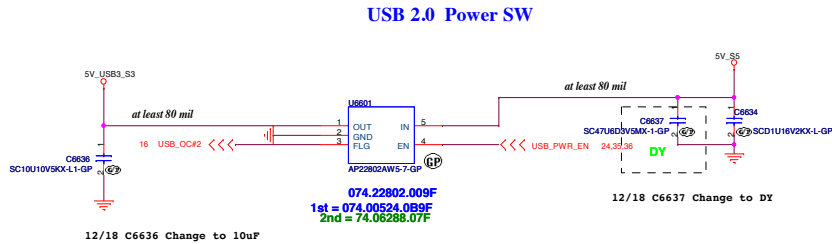
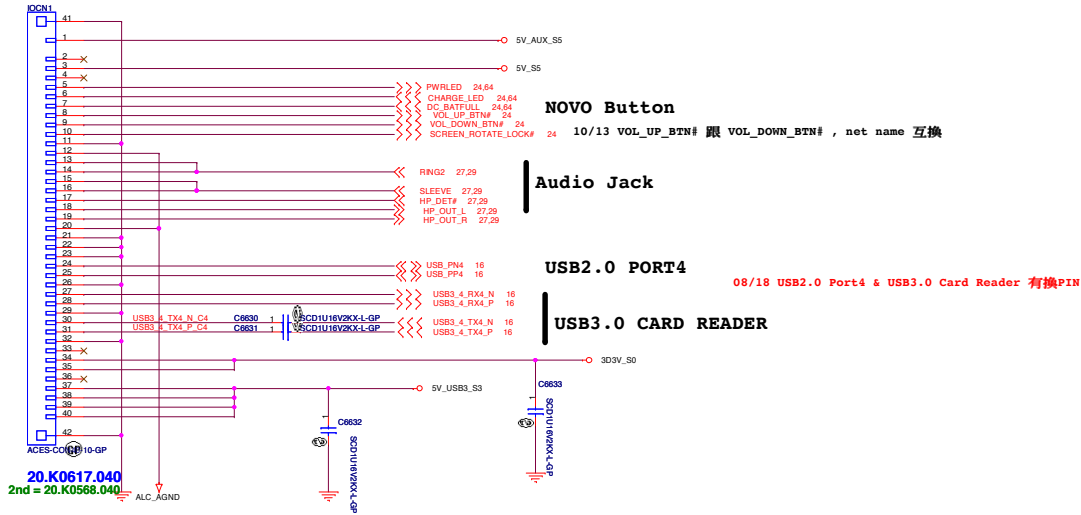
AFTE14P-GP AFTP6403

AFTE14P-GP AFTP6404

AFTE14P-GP AFTP6405

AFTE14P-GP AFTP6406

IO BD Device	
Item	Device
1	NOVO Button
2	Audio Jack
3	USB Card Reader
4	USB2.0 Port4

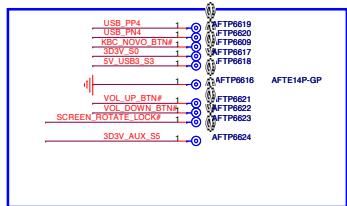


U6301 place near to IOCNI

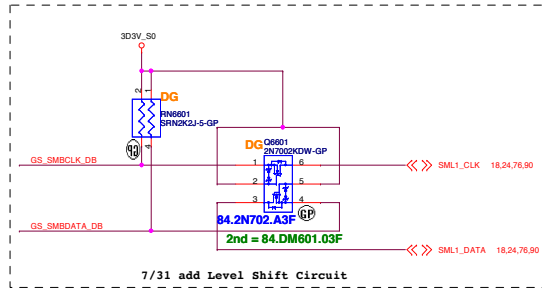
12/18 074.22802.009F 被禁用

08/05 U6601 add 2nd & 3rd Source

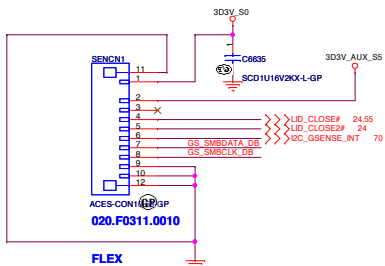
Test point



10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN# , net name 互换



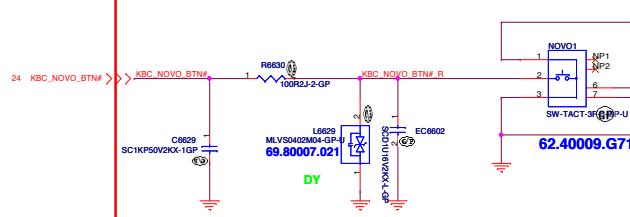
Flex360 SENSOR BD



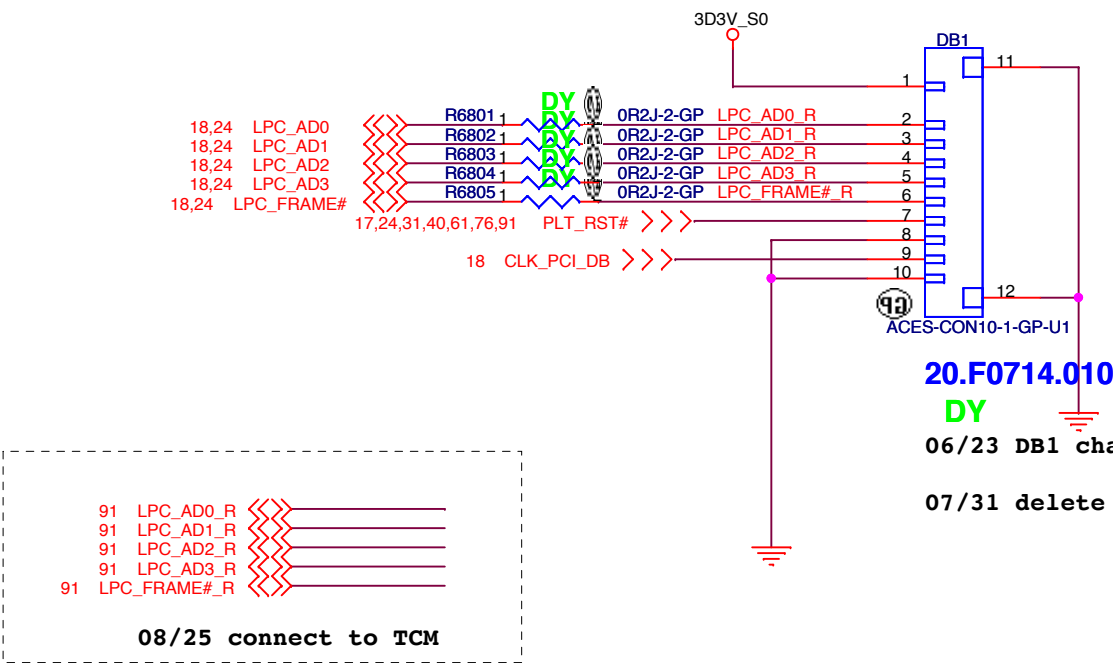
Hall sensor

06/12 Delete Hall Sensor CONN, 換7 pin 與SPK 訊號接同一CONN, SPK1

Novo Button



Debug Connector



20.F0714.010

DY

06/23 DB1 change to Test point

07/31 delete Test point, add Debug CONN

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Dubug connector</i>			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015	Sheet 68 of	102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (2/5)

Size Custom

Document Number

LT41

Rev

-1

Date: Tuesday, January 20, 2015

Sheet 69 of 102

The Slave Address (SA0) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSB is '1' (address 0011001b) else if SA0 pad is connected to ground, LSB value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.

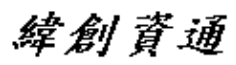


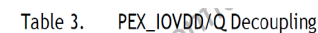
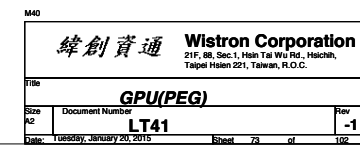


BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Thunderbolt (4/5)			
Size	Document Number	Rev	
Custom	LT41	-1	
Date:	Tuesday, January 20, 2015	Sheet	71 of 102

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (5/5)			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015		Sheet 72 of 102

[illegible]



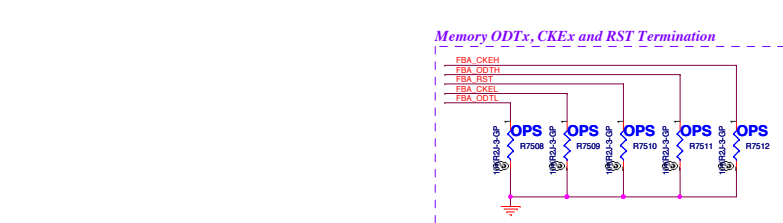
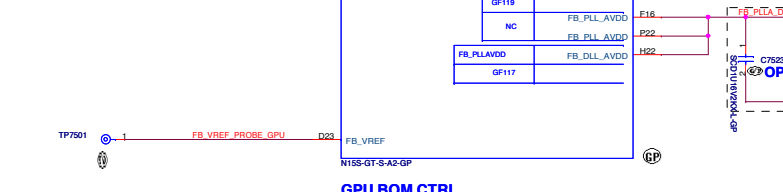
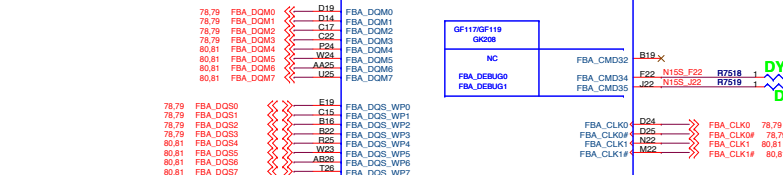
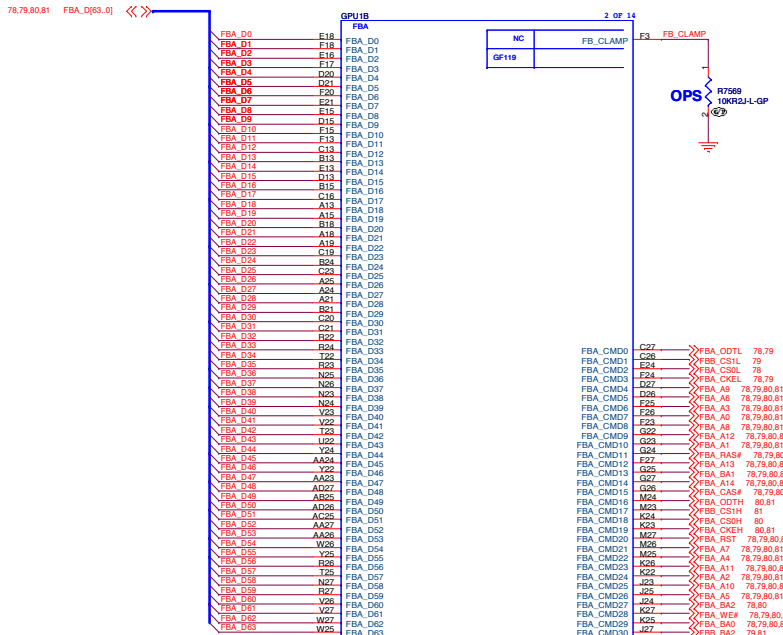


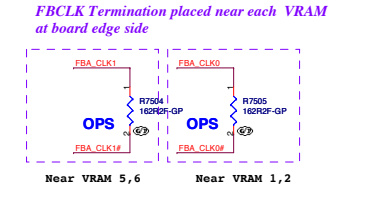
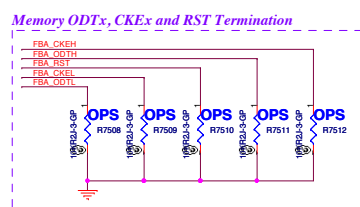
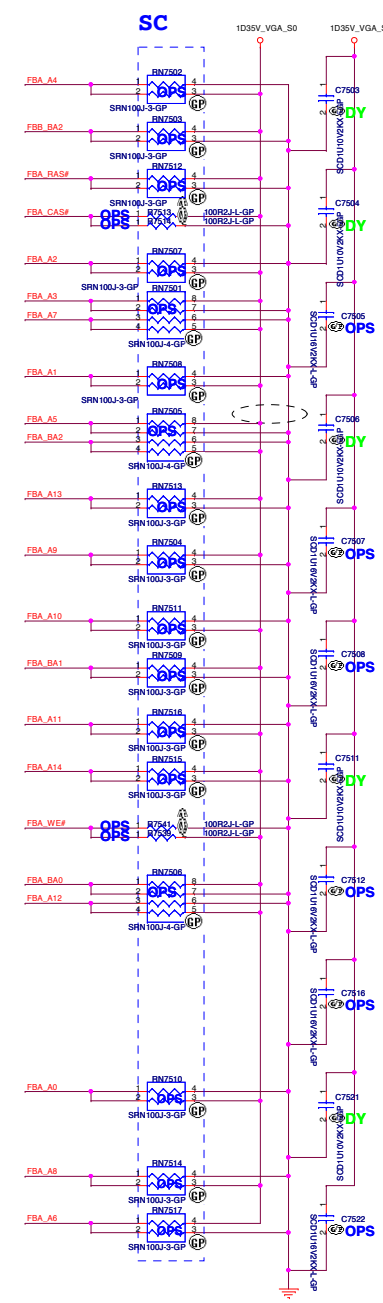
Table 6-4. Mode E Command Mapping

	Rank 0	Rank 1
N15x DDR3 Mode E	Data Bits [1:0]	Data Bits [63:32]
FbxCMD0	QDT	QDT
FbxCMD1	CS0*	CS1*
FbxCMD2	CKE	CKE
FbxCMD3	CS0*	CS1*
FbxCMD4	A9 A9 A9 A9	A11 A11 A11 A11
FbxCMD5	A6 A6 A6 A6	A7 A7 A7 A7
FbxCMD6	A3 A3 A3 A3	BA1 BA1 BA1 BA1
FbxCMD7	A0 A0 A0 A0	A12 A12 A12 A12
FbxCMD8	A8 A8 A8 A8	A8 A8 A8 A8
FbxCMD9	A12 A12 A12 A12	A0 A0 A0 A0
FbxCMD10	A1 A1 A1 A1	A2 A2 A2 A2
FbxCMD11	RA5* RA5* RA5* RA5*	RA0* RA0* RA0* RA0*
FbxCMD12	A13 A13 A13 A13	A14 A14 A14 A14
FbxCMD13	BA1 BA1 BA1 BA1	A3 A3 A3 A3
FbxCMD14	A14 A14 A14 A14	A13 A13 A13 A13
FbxCMD15	CAS* CAS* CAS* CAS*	CAS* CAS* CAS* CAS*
FbxCMD16	QDT	QDT
FbxCMD17	CS1*	CS1*
FbxCMD18	CKE	CKE
FbxCMD19	CS0*	CKE
FbxCMD20	RST RST RST RST	RST RST RST RST
FbxCMD21	A7 A7 A7 A7	A6 A6 A6 A6
FbxCMD22	A4 A4 A4 A4	A5 A5 A5 A5
FbxCMD23	A11 A11 A11 A11	A9 A9 A9 A9
FbxCMD24	A2 A2 A2 A2	A1 A1 A1 A1
FbxCMD25	A10 A10 A10 A10	WE* WE* WE* WE*
FbxCMD26	A5 A5 A5 A5	A4 A4 A4 A4
FbxCMD27	BA2 BA2 BA2 BA2	BA2 BA2 BA2 BA2
FbxCMD28	WE* WE* WE* WE*	A10 A10 A10 A10
FbxCMD29	BA0 BA0 BA0 BA0	BA0 BA0 BA0 BA0
FbxCMD30	BA0 BA0 BA0 BA0	BA2 BA2 BA2 BA2
FbxCMD31		

N15x DDR3 Mode E	Rank 0	Rank 1
FbxCMD34	DBG0 ¹	
FbxCMD35	DBG1 ¹	

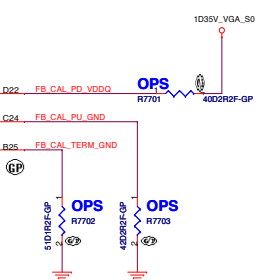
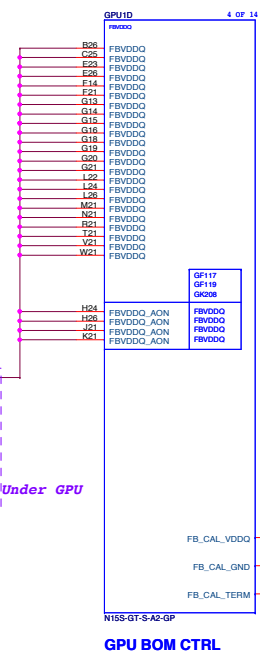
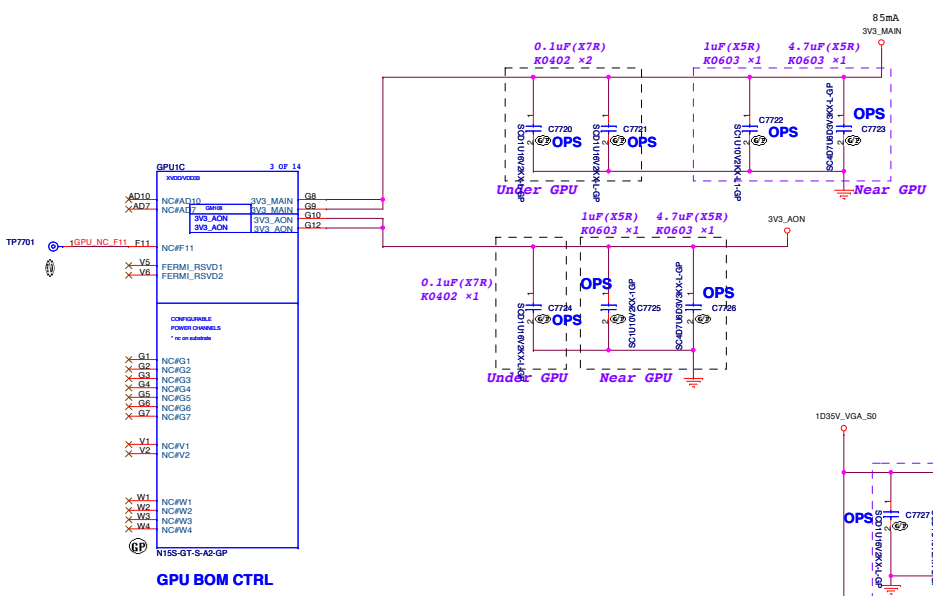
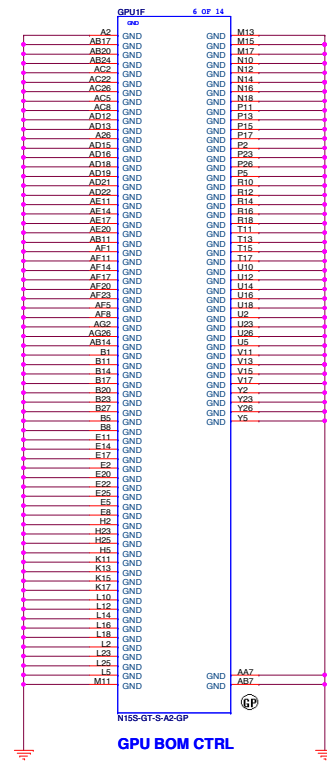
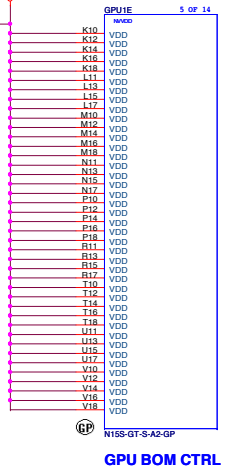
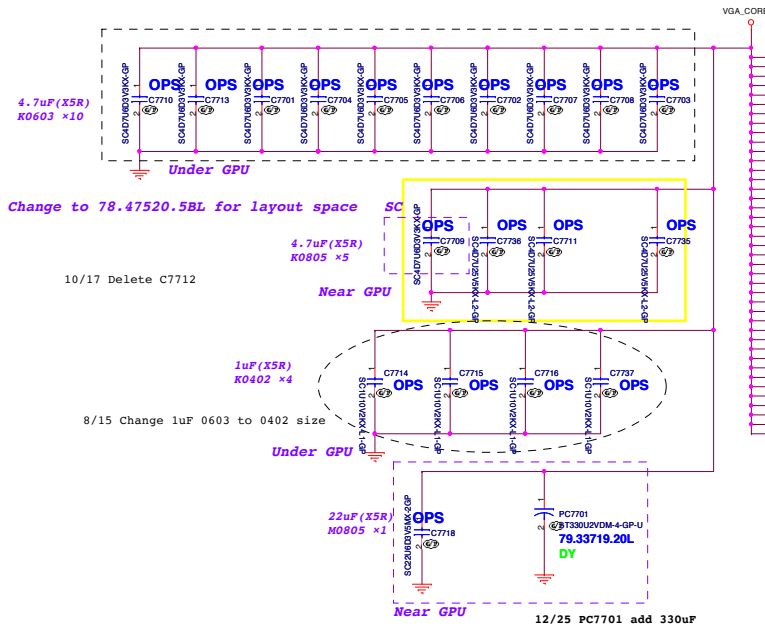
Notes:
1. Not available in GB2-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11

GPU Strap change Res. To Parallel Res.

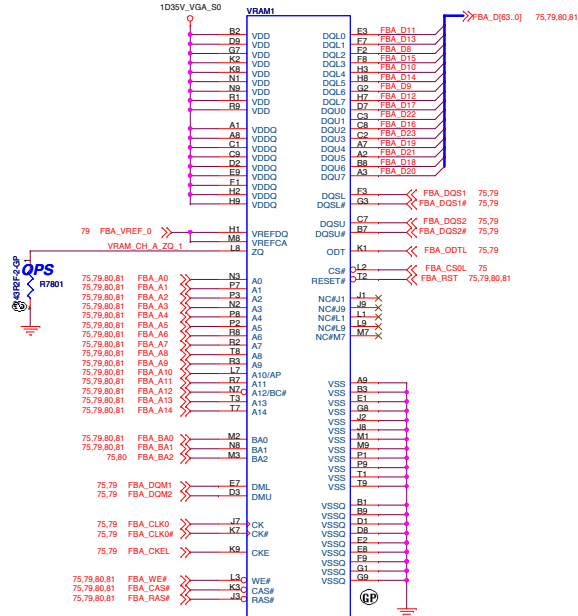




10/16 GPU PN change to 071.GM108.000U

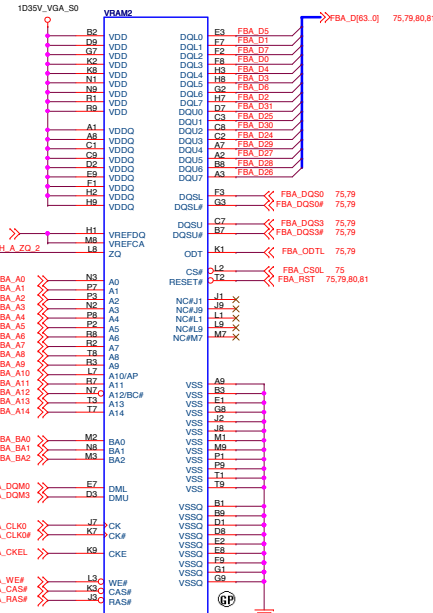


Data Bits 31:0 RANK 0

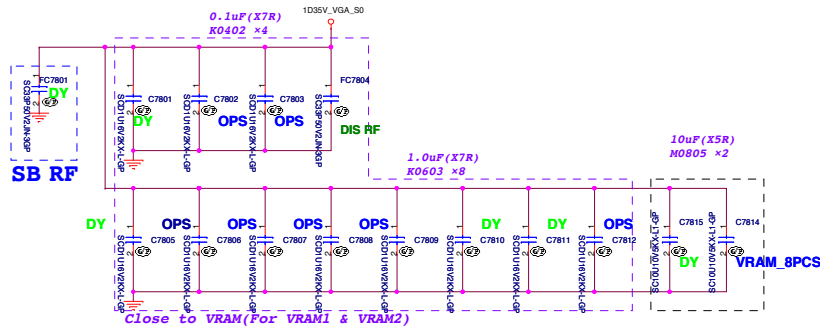


HSTC463AFR-11C-GP
72.05463.D0U
VRAM BOM CTRL

10/23 VRAM1-VRAM8 Part Number 72.05463.D0U

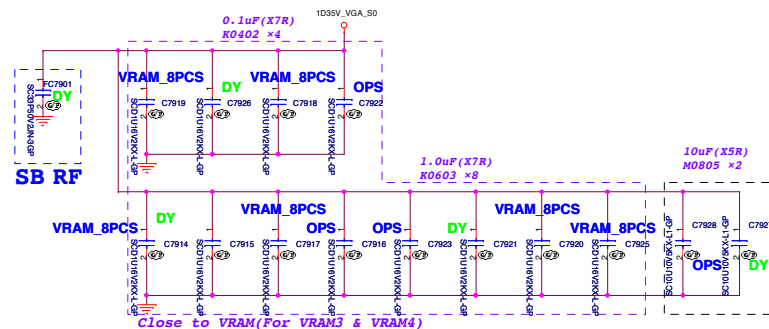
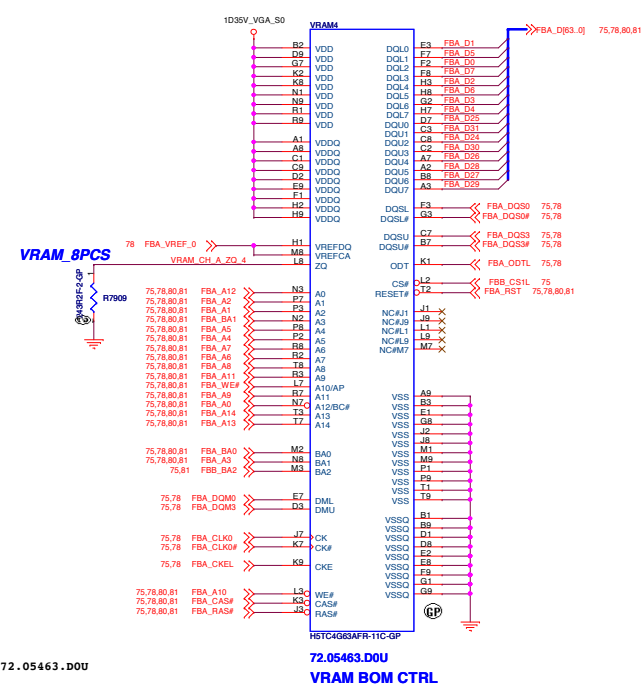
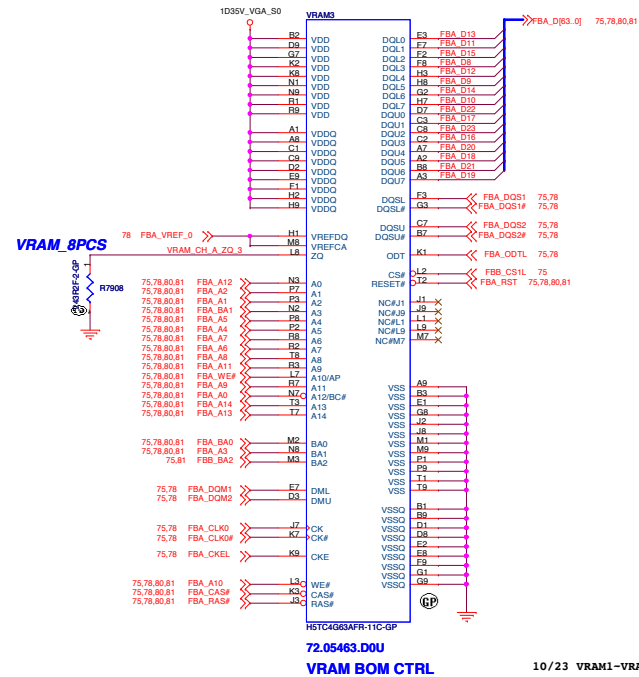


HSTC463AFR-11C-GP
72.05463.D0U
VRAM BOM CTRL



08/18 C7801, C7804, C7805, C7810, C7811 Change to DI

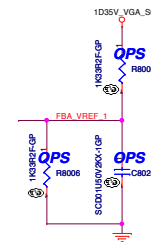
08/18 C7814 Change to VRAM_8PCS

Data Bits 31:0 RANK 1

08/18 C7915, C7921, C7926 Change to DY

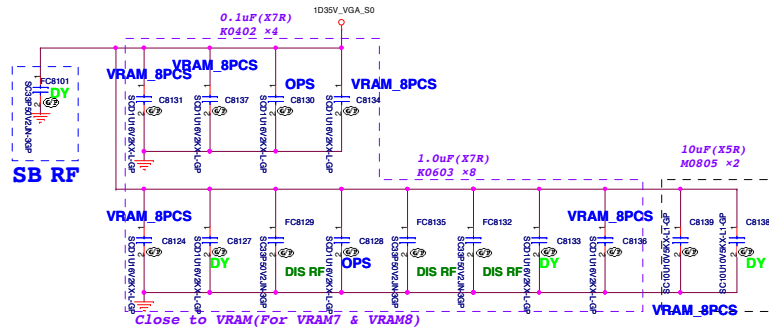
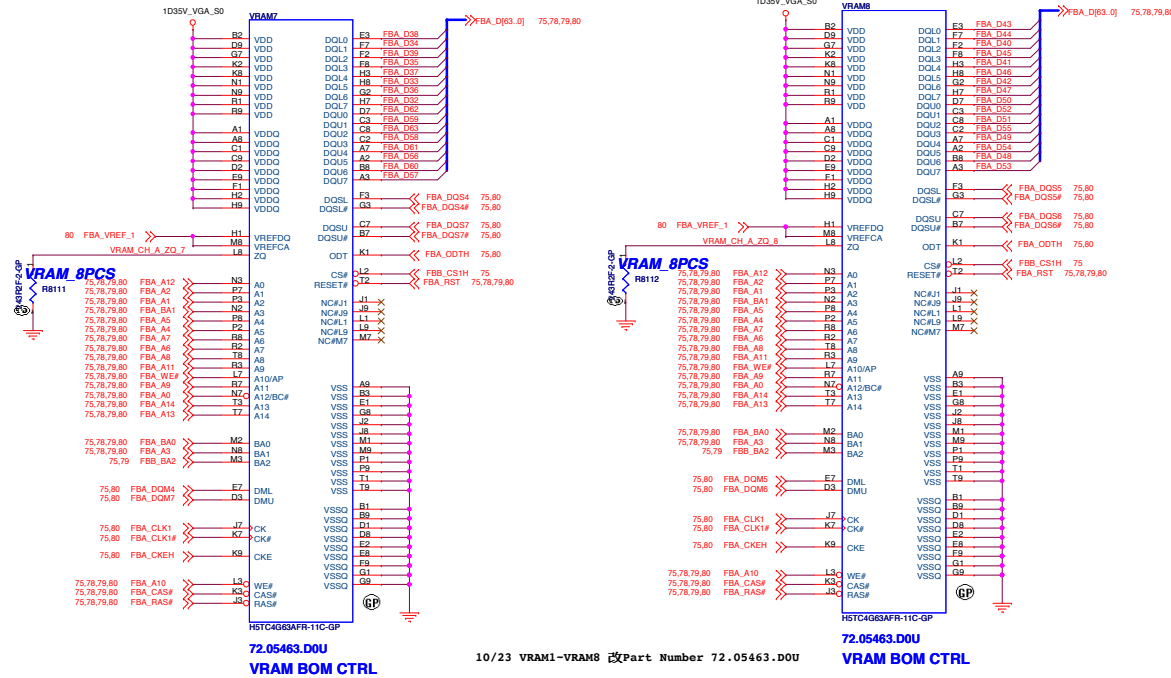
08/18 C7914, C7917, C7918, C7919 ,C7920, C7925 Change to VRAM_8PCS

10/23 VRAM1-VRAM8 改 Part Number 72.05463.D0U



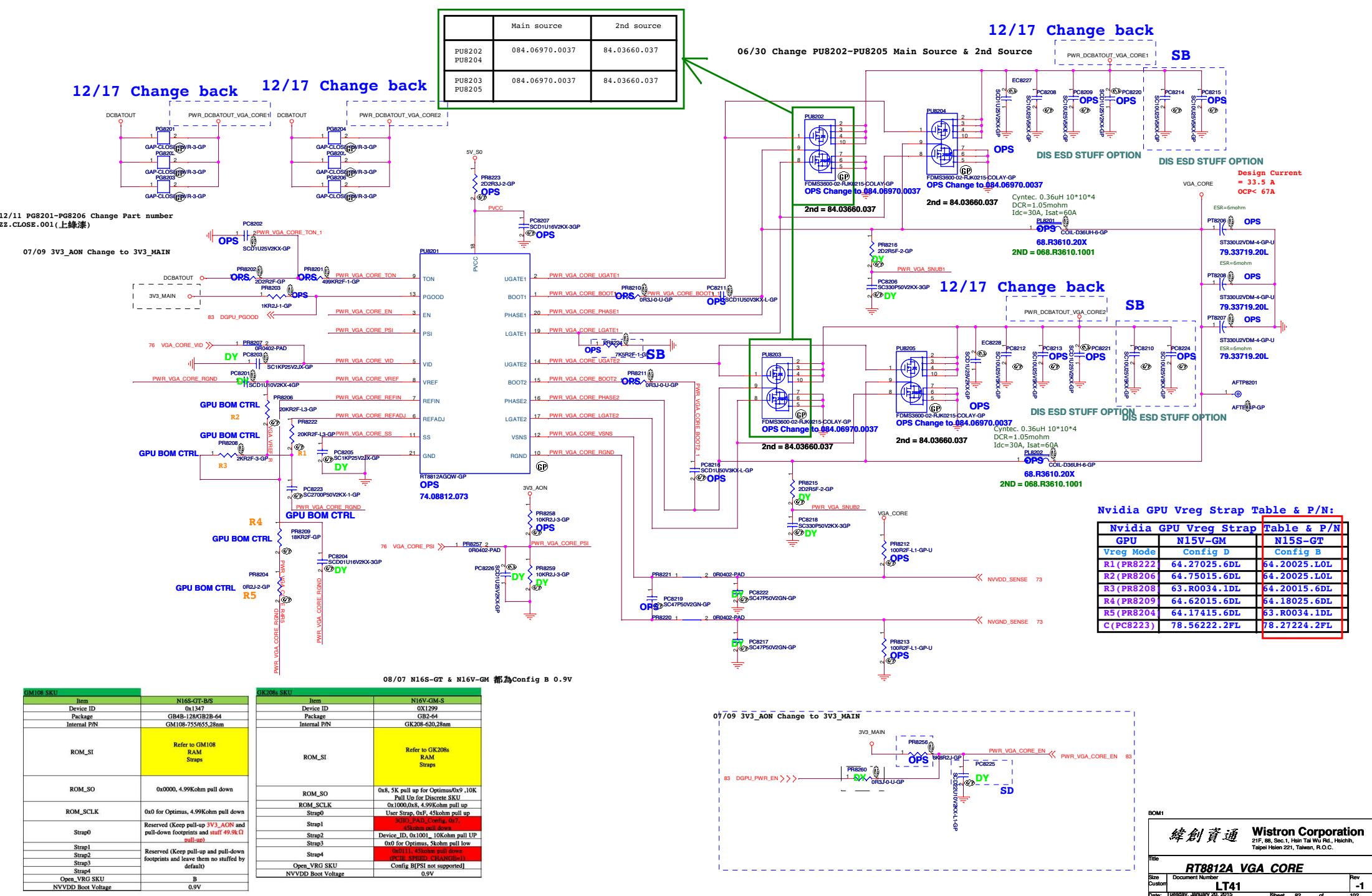
08/18 C8021 Change to VRAM_8PCS

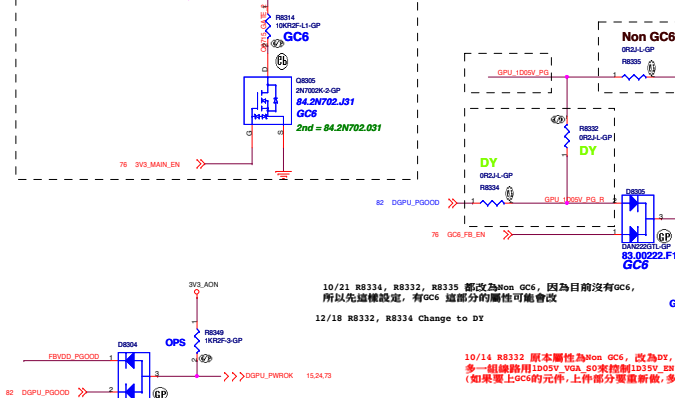
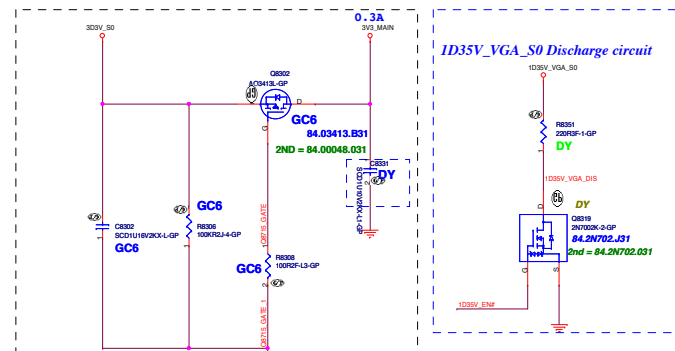
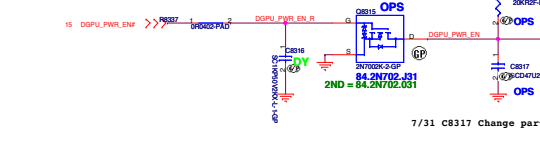
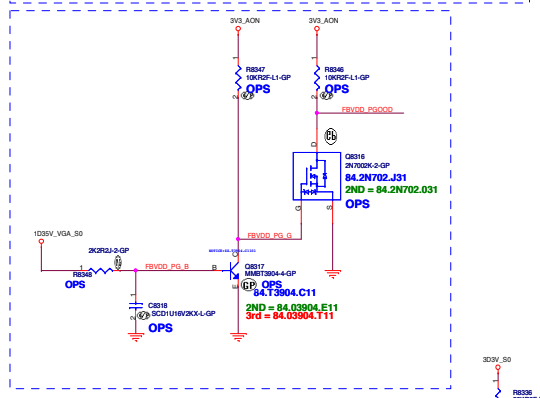
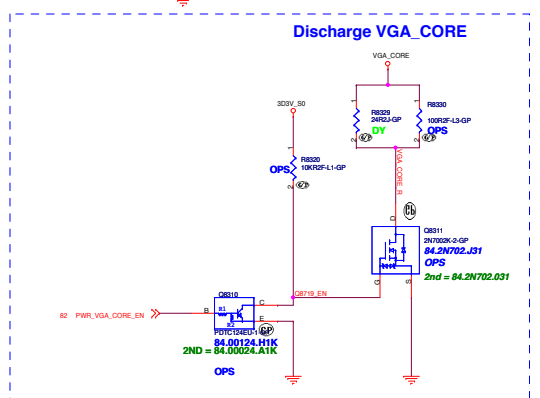
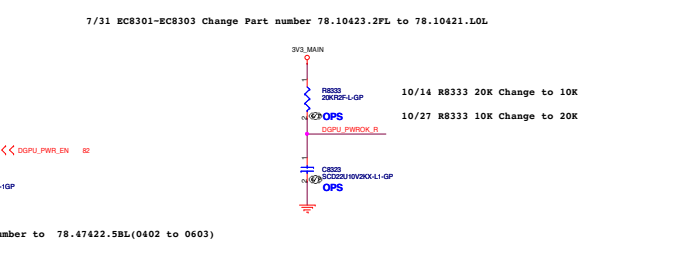
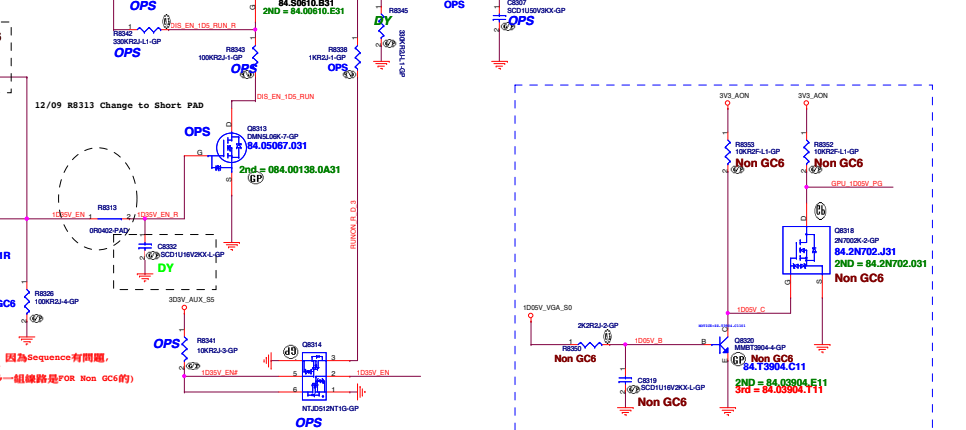
Data Bits 63:32 RANK 1



08/18 C8127, C8129, C8132, C8133, C8135 Change to DY

08/18 C8124, C8131, C8134, C8136, C8137, C8139 Change to VRAM_8PCS



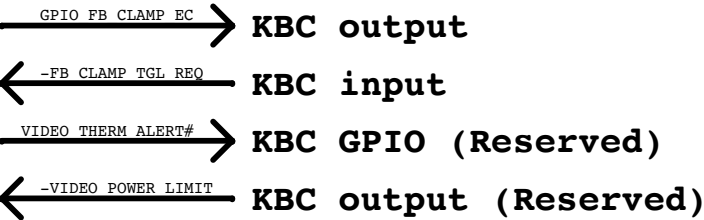
[illegible][illegible][illegible]

10/14 多一組線路用1D05V_VGA_50來控制1D35V_EN
(如果要上GC6的元件,上件部分要重新做,多一組線路是FOR Non GC6的)
10/21 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to DY
(原本為Non GC6)
12/18 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to STUFF

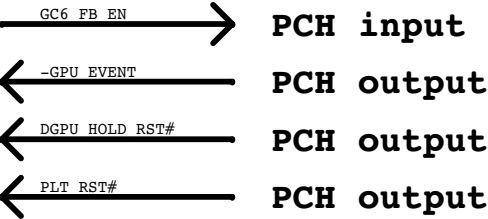
12/11 PG8316-PG8319 Change Part number
ZZ.CLOSE.001(上縁漆)

Undefined Sys <--> GPU IO

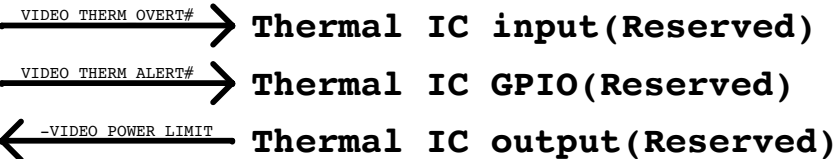
KBC <--> GPU



PCH <--> GPU



Thermal IC <--> GPU

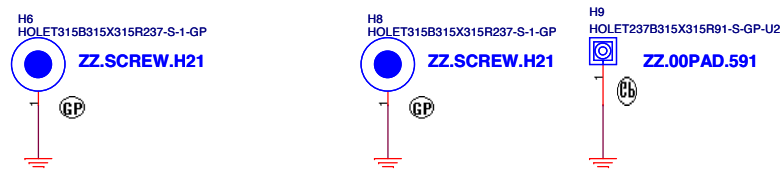


BOM1

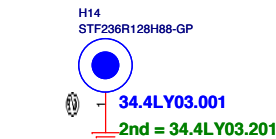
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Switchable GFX LCD(2/2)		
Size	Document Number	Rev
A4	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 85 of 102

08/14 H6, H8 ZZ.00PAD.591 Change to ZZ.SCREW.H21

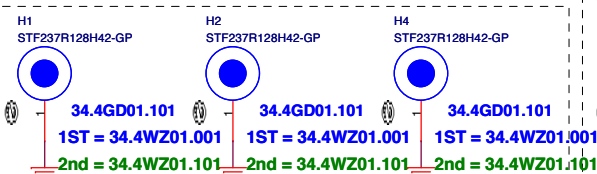
Structure boss



Stand off

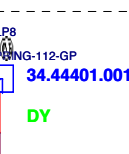
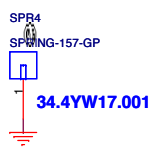
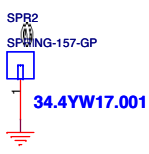
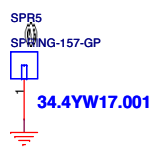
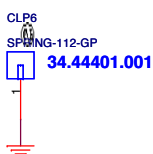
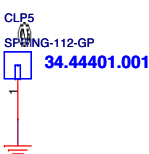
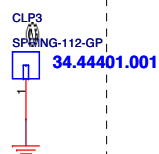
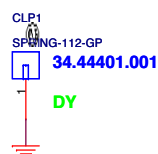
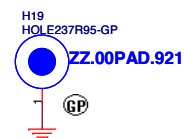
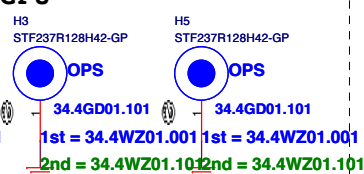


CPU



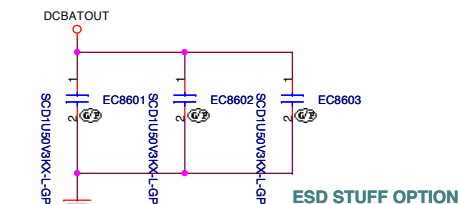
07/29 H3 Change to OPS

GPU

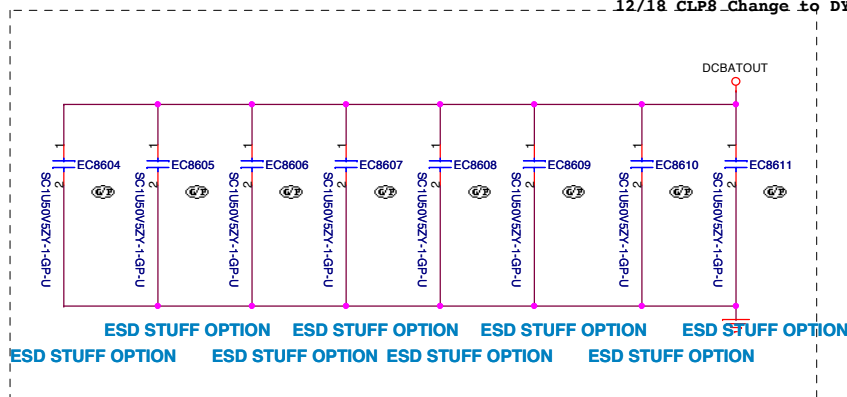


06/06 Delete Clp3 記得SB版要將CLP 上件
10/22 CLP1, CLP4, CLP7, CLP8 上件(原本為ZZ)
10/22 SPR1 上件(原本為ZZ)
12/18 CLP1 Change to DY
12/18 Delete CLP4, 因為那位置要放SPR4

01/13 add SPR5 08/22 add SPR2
06/18 add SPR1 12/11 SPR2 改上件 10/20 add CLP7, CLP8
12/23 Delete SPR1 10/17 add EC8604-EC8611 for EMI 10/23 Delete CLP7
12/18 CLP8 Change to DY



06/25 add EC8601, EC8602, EC8603

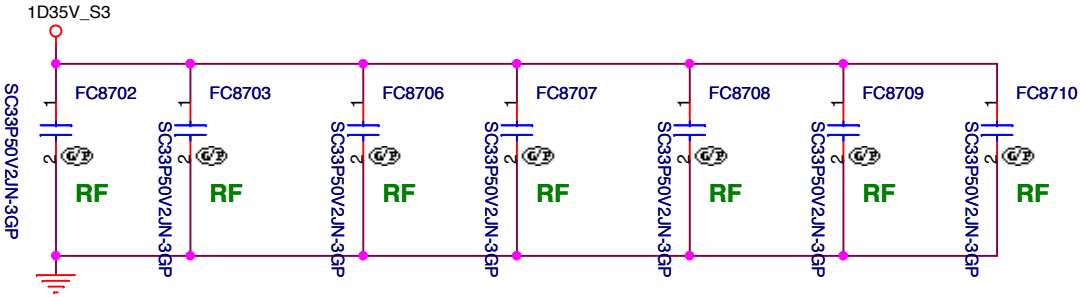
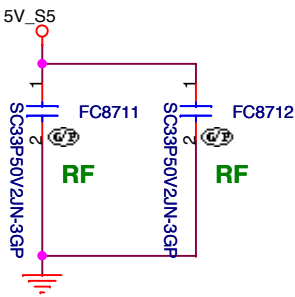
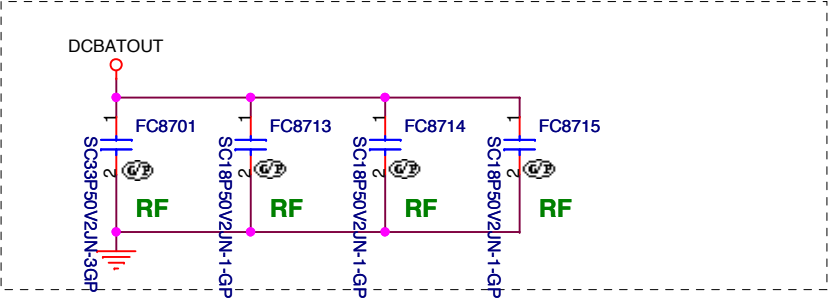


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors		
Size A3	Document Number	LT41	Rev -1
Date:	Tuesday, January 20, 2015	Sheet 86 of 102	

10/19 add for RF



10/23 Delete FC8704,FC8705

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

Document Number

Rev

LT41

-1

Date: Tuesday, January 20, 2015

Sheet 87 of 102

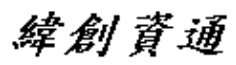
5	4	3	2	1
D				D
C				C
B				B
A				A

WWW.ALISALER.COM

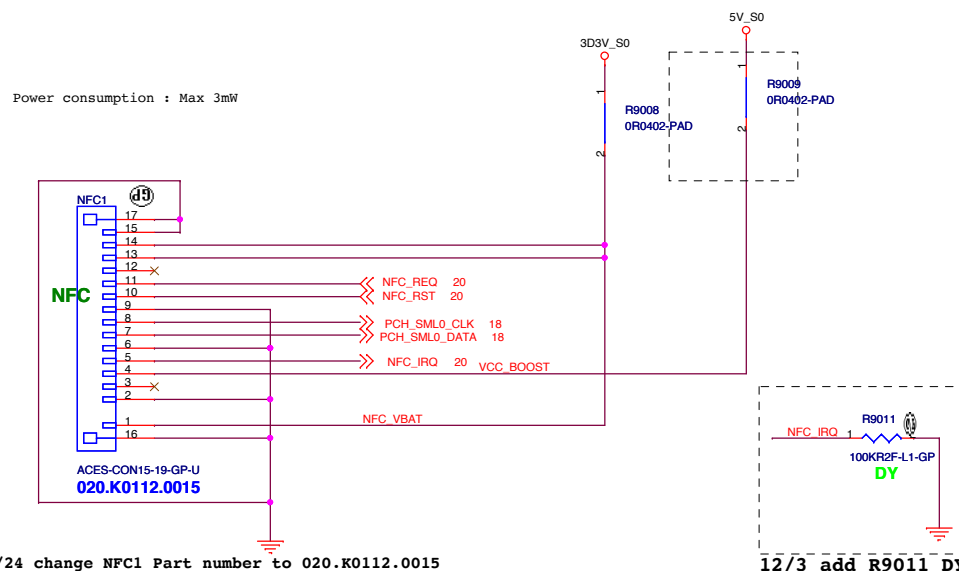
BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet	88 of 102

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Finger Print			
Size A4	Document Number LT41		Rev -1
Date: Tuesday, January 20, 2015		Sheet 89 of	102

07/03 add R9009 5V_S0 Connect to NFC CONN Pin12 (SA板 未接)

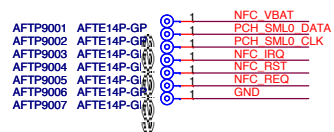


08/24 change NFC1 Part number to 020.K0112.0015

08/25 020.K0112.0015 新CONN, Pin腳整個反過來

07/07 add R9010 Connect to GND

07/21 Delete R9010 Connect to GND



Pin#	Pin Name	Type	Refer	Description
1	VBAT	power	3.3V	Power supply voltage
2	GND	Power	GND	Ground
3	SWP	IO	-	SIM Card data
4	VCC_BOOST	Power	5V	Booster supply
5	IRQ	O	PVDD	Interrupt
6	PMUVCC	Power	connect to outside SE power or GND (no SE)	UICC power input from external PMU
7	I2C_SDA	I/O	PVDD	I2C Serial Data Line
8	I2C_SCL	I/O	PVDD	I2C Serial Clock Line
9	GND	Power	GND	Ground
10	VEN	I	GPIO Control (Normal 3.3V)	Enable/ disable LDO regulator / Reset
11	DWL_REQ	I	GPIO Control (Normal 0V)	Firmware download control pin
12	SIMVCC	Power	1.8V or N.C	Power output to supply the UICC
13	VBAT	Power	3.3V	Power supply voltage
14	PVDD	Power	3.3V	Pad supply voltage
15	GND	Power	GND	Ground

15 GND Power GND Ground 1

WWW.ALISALER.COM

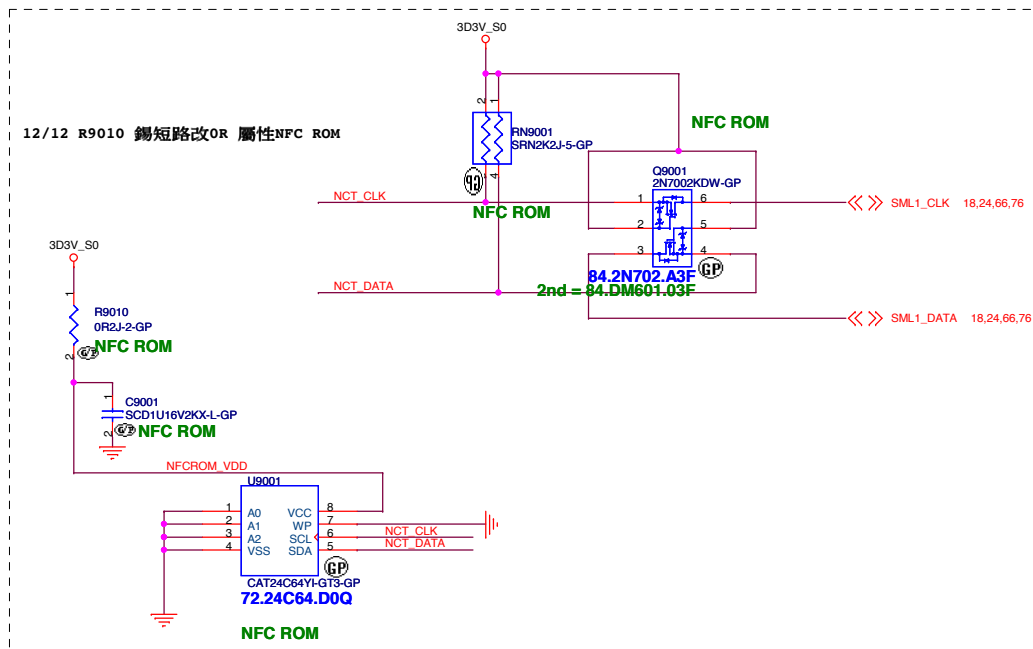
12/3 add R9011 DY

NFC Module Pin Define



Suggestion Host Pin define Use Sinbon FFC A9152420)

Pin#	Pin Name
15	VBAT
14	GND
13	SWP
12	VCC_BOOST
11	IRQ
10	PMUVCC
9	I2C_SDA
8	I2C_SCL
7	GND
6	VEN
5	DWL_REQ
4	SIMVCC
3	VBAT
2	PVDD
1	GND



10/15 增加線路

10/15 U9001 料號記得要帶對,目前的不是要用的

10/16 NFC ROM都不上件,待驗證

BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

NFC

Size

Document Numl

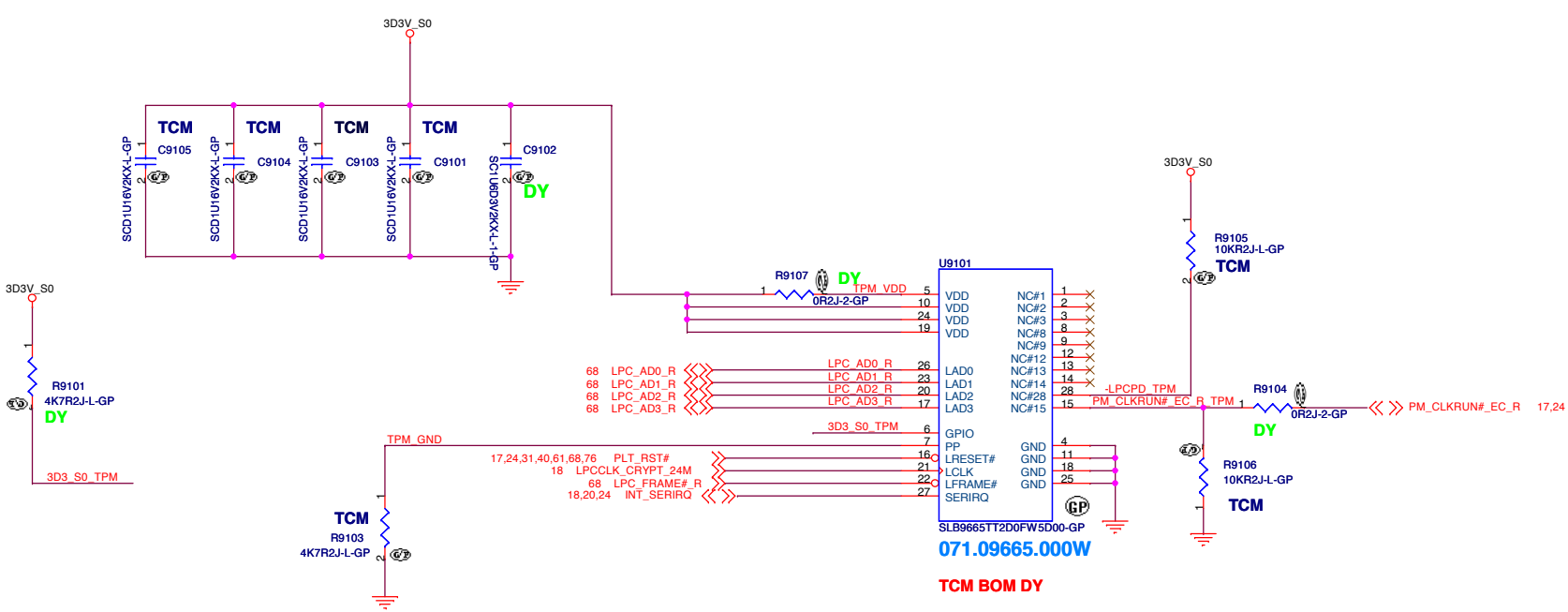
LT41

Date: Tuesday, January 20, 2015

Sheet 9

-1

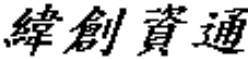
102



06/10 國民IC Pin5, Pin6 NC
Pin 15 GND

06/25 因國民的IC, 還未有料號,所以先要SAMPLE,回來自己上件

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Switchable GFX eDP			
Size A	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015	Sheet	92 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

WWW.ALISALER.COM

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>Bottom Docking</div>			
<div>Size</div> <div>A</div>	<div>Document Number</div> <div>LT41</div>		<div>Rev</div> <div>-1</div>
<div>Date:</div> <div>Tuesday, January 20, 2015</div>	<div>Sheet</div> <div>93</div>	<div>of</div> <div>102</div>	

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Inter LAN WG1217LM		
Size	Document Number	Rev
A3	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 94 of 102

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN Switch			
Size	Document Number		Rev
A	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet	95 of 102

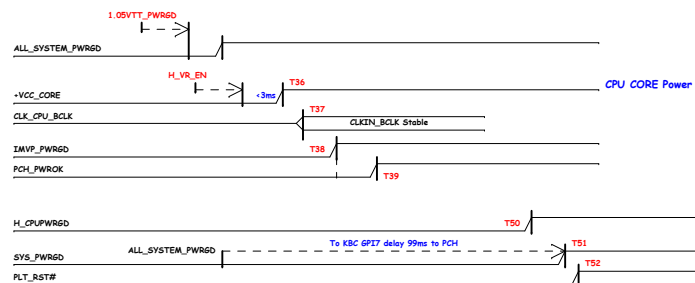
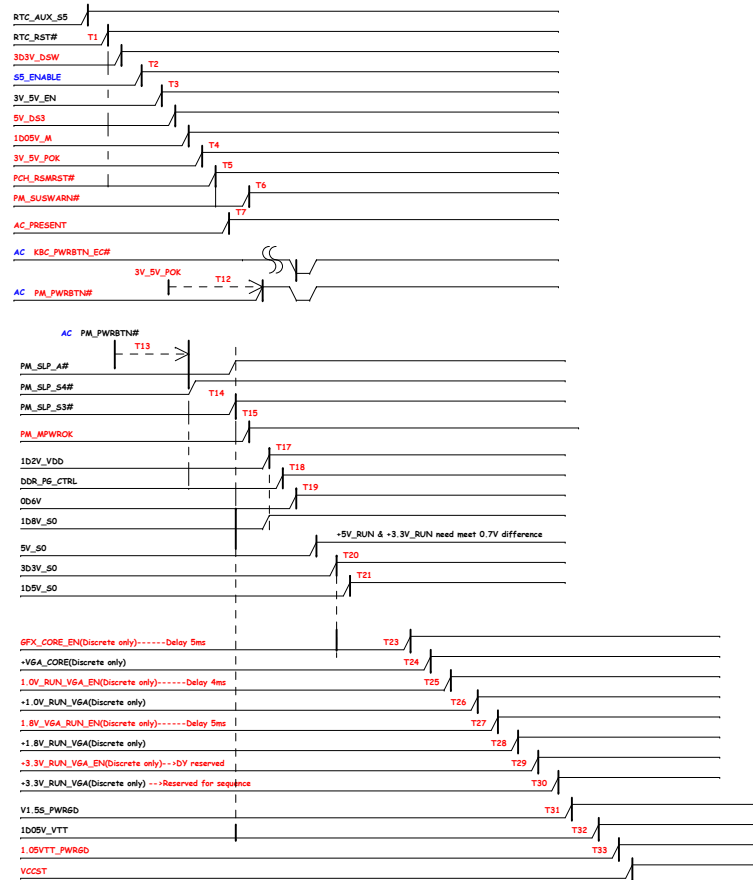
BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
PCH XDP		
Size	Document Number	Rev
A4	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 96 of 102

GPU BOM CTRL		
For Detail see P82		
GPU	N16V-GM	N16S-GT
Lenovo P/N	071.0N16V.000U	071.0N16S.000U
OPS (UMA:DX)	V	V
PR8222	64.20025.L0L	64.20025.L0L
PR8206	64.20025.L0L	64.20025.L0L
PR8208	64.20015.6DL	64.20015.6DL
PR8209	64.18025.6DL	64.18025.6DL
PR8204	63.R0034.1DL	63.R0034.1DL
PC8223	78.27224.2FL	78.27224.2FL

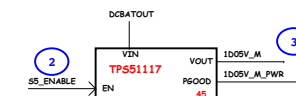
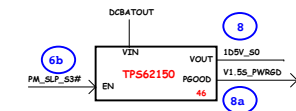
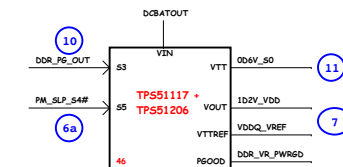
VRAM BOM CTRL (Default Setting:900MHZ)									
Lenovo P/N		1101018	1100788	1100897	1101028	1101019	1100661	1100677	
IC Vendor		Micron	Hynix	Hynix	Samsung	Samsung	Micron	Micron	
IC Vendor P/N		MT41J256M16HA-093G:E N15S-GT only	H5TC2G63PFR-11C N15V-GM/N15S-GT	H5TC4G63APR-11C N15V-GM/N15S-GT	K4W2G1646Q-BC1A N15V-GM/N15S-GT	K4W4G1646D-BC1A N15V-GM/N15S-GT	MT41J128M16JT-093G:K N15S-GT only	MT41K256M16HA-107G:E N15V-GM only	
RAM0 VRAM1, VRAM2, VRAM5, VRAM6		Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 1GB	
RAM1 VRAM3, VRAM4, VRAM7, VRAM8		Stuff with Discrete 4GB		Stuff with Discrete 4GB		Stuff with Discrete 4GB			
R7642(Strap0-L)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L				
R7631(Strap0-H)		N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N16S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	
R7643(Strap1-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DL		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7632(Strap1-H)					N15V-GM:64.10025.L0L				
R7644(Strap2-L)						N15V-GM:64.10025.L0L			
R7633(Strap2-H)			N15V-GM:64.10025.L0L	N16V-GM:64.10025.L0L	N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L	
R7645(Strap3-L)				N16V-GM:64.49915.6DL					
R7635(Strap3-H)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7646(Strap4-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7634(Strap4-H)									
R7639(ROM_SI-L)		N15S-GT:64.24925.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.20025.L0L	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7636(ROM_SI-H)			N15S-GT:64.10025.L0L		N15S-GT:64.20025.L0L		N15S-GT:64.15025.6DL		
R7640(ROM_SO-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7637(ROM_SO-H)				N16V-GM:64.49915.6DL			N15S-GT:64.49915.6DL		
R7641(ROM_SCLK-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7638(ROM_SCLK-H)				N16V-GM:64.49915.6DL			N15S-GT:64.49915.6DL		

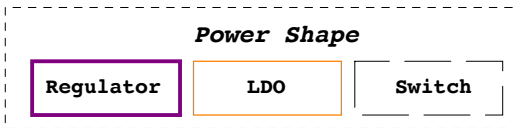
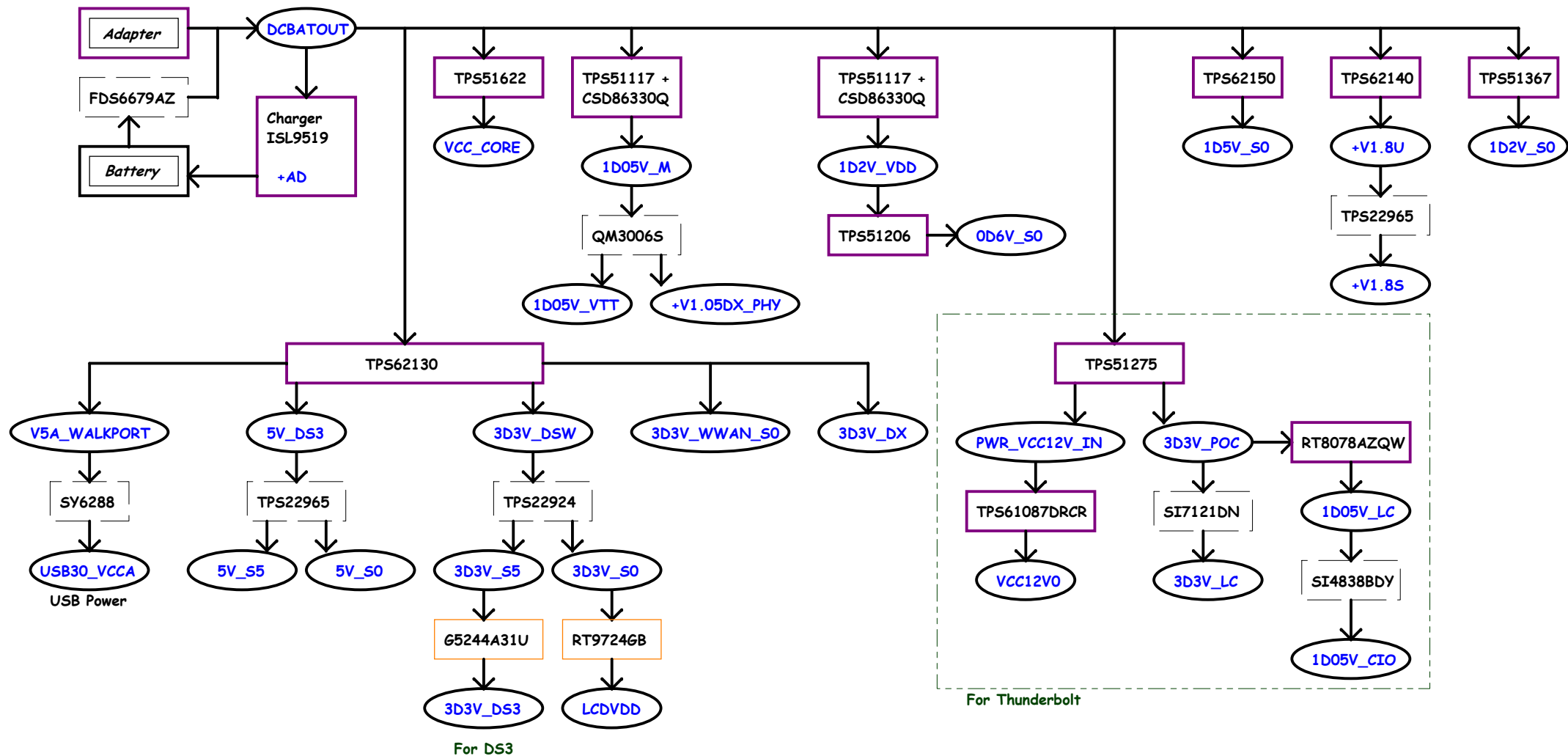
(AC mode)



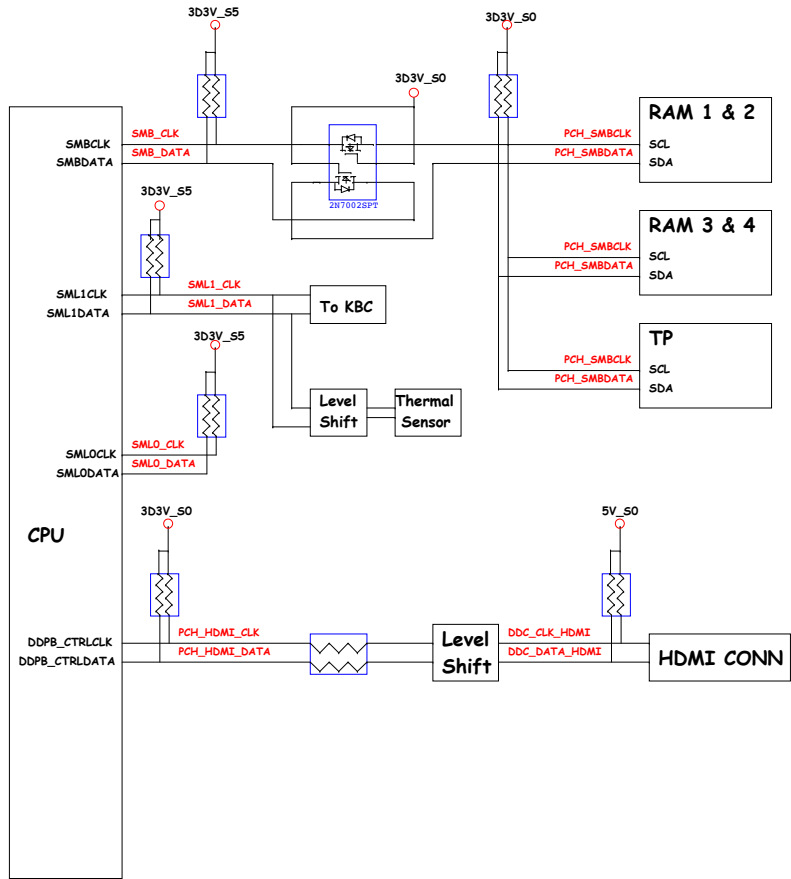
The schematic diagram illustrates the power management system for the Shark Bay CPU. It shows the power flow from an AC Adapter (38) and DC Battery (32) through various regulators and switches (1-18) to the Shark Bay CPU. Key components include the I2L9519 Charger (40), KBC IT8587 (6), PCH (17), and VR TP51622 (12). The diagram is annotated with callouts 1 through 18, corresponding to the table below.

Callout	Component	Part Number	Notes
1	AC Adapter	38	
1a	SWITCH	40	
1b	I2L9519 Charger	40	
1c	DC Battery	32	
2	TP562130 (3D3V_DS#)	41	
2	TP562130 (5V)	41	
2	TP562130 (5V)	41	
3	TP562130 (5V)	41	
4	TP562130 (5V)	41	
5a	KBC	IT8587	
5b	PCH		
5c	PCH		
6	KBC	IT8587	
7	PCH		
8	PCH		
9	PCH		
10	VR	TP51622	
11	VR	TP51622	
12	VR	TP51622	
13	VR	TP51622	
14	SWITCH	36	
15	SWITCH	36	
16	SWITCH	36	
17	PCH		
18	PCH		

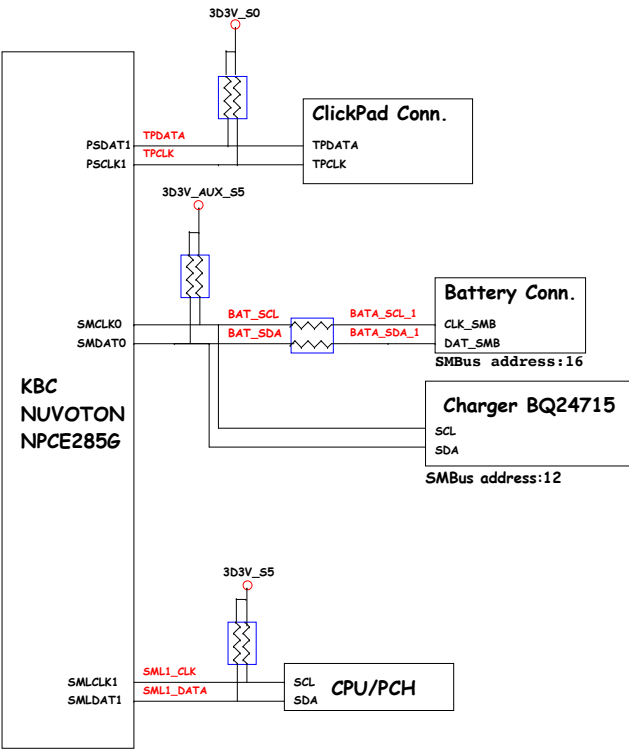




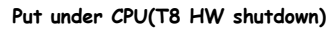
CPU/PCH SMBus Block Diagram



KBC SMBus Block Diagram



WWW.ALISALER.COM



The diagram illustrates the internal connections of the ALC233 codec. On the left, the codec is represented by a vertical bar with labels for its pins. On the right, external components are shown in boxes. The connections are as follows:

- SPK-OUT-L-** and **SPK-OUT-L+** connect to a **SPEAKER** box.
- SPK-OUT-R-** and **SPK-OUT-R+** connect to another **SPEAKER** box.
- HPOUT-L/PORT-T-L** and **HPOUT-R/PORT-T-R** connect to a network of resistors, which then connects to the **HP OUT** box.
- MIC2-L/PORT-F-L** and **MIC2-R/PORT-F-R** connect to a network of resistors and a capacitor, which then connects to the **HP OUT** box.
- SENSE_A** connects to the **HP OUT** box.
- MIC1-L/PORT-B-L** and **MIC1-R/PORT-B-R** connect to a network of resistors and a capacitor, which then connects to the **MIC IN** box.
- SENSE_A** connects to the **MIC IN** box.
- DMIC-CLK** and **DMIC-DATA** connect to the **DMIC** box.